Performance Limits of Fractional-N Digital PLLs with Mid-Rise TDCs

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2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME) | 979-8-3503-0320-9/23/$31.00 ©2023 IEEE | DOI: 10.1109/PRIME58259.2023.10161782

***Abstract*—Fractional-N digital phase-locked loops (DPLL's) typically use a multi-stage noise-shaping (MASH) digital Δ-Σ modulator (DDSM) divider controller to synthesize an output frequency that is a non-integer multiple of the reference. The quantization error (QE) arising from the divider controller, if not being canceled prior to reaching the time-to-digital converter (TDC), can overwhelm the TDC input jitter level and in turn deteriorate the phase noise (PN) of the TDC, and hence that of the DPLL at the system level. This sets a performance limit for such DPLLs, for which case it is crucial to predict explicitly the worst-case output PN in order to analyze fractional-N PN mitigation techniques critically. This paper investigates this scenario, for which the input jitter analysis and output PN prediction are performed. Multi-rate discrete-time behavioral simulation at the system level confirms the accuracy of our analytical predictions.**

***Index Terms*—digital phase locked loop (DPLL), fractional-N, bang-bang, jitter, linear analysis, frequency synthesizer, delta-sigma modulation, MASH, DDSM, TDC, DTC, PLL.**

I. Introduction

A fractional-N digital phase-locked loop (DPLL) such as that shown in Fig. 1 uses a multi-stage noise-shaping (MASH) digital Δ-Σ modulator (DDSM), commonly of order greater than one, e.g., MASH 1-1 or 1-1-1, to control the multi-modulus divider (MMD) in the feedback path in order to produce an output frequency that is a non-integer multiple of the reference frequency. Switching from the integer-N mode to the fractional-N mode, the quantization error (QE) arising from the divider controller presents at the input of the time-to-digital converter (TDC), and is more significant than the input jitter contributed by the intrinsic noise/jitter sources [1]. This reduces the linearized gain of the TDC drastically due to the dependency of the TDC gain on the statistical properties of the input jitter [2]. Intuitively, this can be understood as the result of the TDC's input range being increased, whilst the output range of the TDC saturates to its top and bottom quantization levels. Consequently, apart from the contribution from the DDSM noise, the suppressed effective gain severely degrades the output phase noise (PN) performance in the locked state [3]. We regard this scenario as a *lower* performance limit of a fractional-N DPLL, because it produces a worst-case output PN.

This publication has emanated from research supported in part by Science Foundation Ireland under Grant number 20/FFP-A/8371 and by Enterprise Ireland under Grant number TC-2015-0019.

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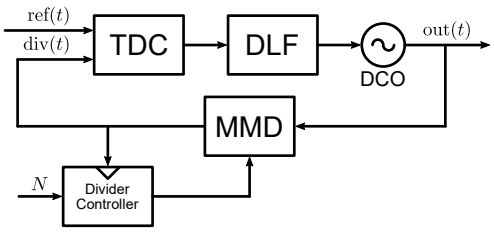

Fig. 1. Fractional-N DPLL system model.

Advanced fractional-N DPLLs typically use techniques such as a digital-to-time converter (DTC) [3] to mitigate the divider controller noise prior to the TDC in order to maintain the loop dynamic optimized for the output PN. Ideally, a DTC with a linear gain can cancel the DDSM noise entirely to recover an integer-N PN, which can be regarded as the theoretical *upper* performance limit of the fractional-N DPLL. However, in reality, the DTC exhibits nonidealities such as quantization and polynomial nonlinearities, and hence can only mitigate the output PN to a level between the lower and upper performance limits. It is useful to derive explicit predictions for these performance limits in order to analyze the effectiveness of techniques to mitigate fractional-N nonlinearity-induced PN and spurs.

Analysis of an integer-N DPLL, corresponding to the "upper limit" in this paper, has been widely studied in the literature, e.g., [4]–[7]. To date, Avallone *et al.* [6] have provided the most accurate prediction for the input jitter and output PN based on a discrete-time system model. However, the scope of their work is limited to the integer-N operation. Fractional-N PN prediction is discussed briefly by Xu and Abidi [7]. However, due to the continuous-time nature of the model used in [7], it lacks accuracy in terms of PN prediction [6]. More importantly, [7] determines the fractional-N TDC gain as a function of the root-mean-square (RMS) input jitter assuming that the DDSM-QE-dominated input jitter is Gaussian distributed; this assumption is incorrect [8]. We have provided an improved TDC linearized analysis that takes into account the interaction between the TDC characteristic and the special distribution of the accumulated DDSM QE [2]. Furthermore, both [6] and [7] are limited to the analysis of a bang-bang DPLL (BBDPLL) with a binary (or bang-bang) phase detector (BPD). PN prediction in the case of fractional-N DPLLs using a generic multi-bit TDC, i.e., the "lower limit", is as yet unreported.

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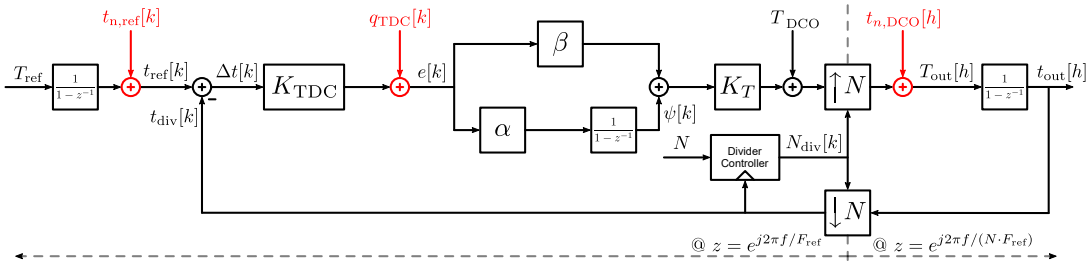

Fig. 2. z-domain model of a multi-rate discrete-time fractional-N DPLL system. The injected noise/jitter sources are marked red.

This paper compares the PN performance limits when the same DPLL operates in its integer-N and fractional-N modes. We adopt the multi-rate discrete-time modeling framework of [6] and extend it to analyze the DPLL with a multi-bit TDC operating in fractional-N mode, a case where the input jitter transfer mechanism is studied for the first time. Together with the linearized analysis of the TDC, a linearized system model and output PN prediction are presented. The predicted PN, taking into account the contributions from reference clock jitter, TDC QE, DCO period jitter, and DDSM QE, is verified by the behaviorally simulated counterpart.

II. Input Jitter Transfer Mechanism and TDC Linearized Analysis

The input jitter analysis starts with the multi-rate z-domain model shown in Fig. 2 for the fractional-N DPLL, which indexes the timestamps of the positive zero-crossing events for the slow-domain signals with k and those for the fast-domain signals with h. Details of the time-stamping method can be found in [2]. As per the model, a recurrent equation for the timestamp of the divided signal can be expressed as

$$t_{\text{div}}[k+1] = t_{\text{div}}[k] + \sum_{h=N_{\text{div}}[k]\cdot k+1}^{N_{\text{div}}[k]\cdot(k+1)} \Bigg\{ \underbrace{K_T\left(\beta\cdot e[k] + \psi[k]\right)}_{\text{control via DLF}} + \underbrace{T_{\text{DCO}} + t_{n,\text{DCO}}[h]}_{\text{DCO period with jitter}} \Bigg\}, \quad (1)$$

where $N_{\text{div}}[k]$ is the instantaneous divide ratio of the kth cycle, K_T is the DCO time gain, $e[k]$ is output from the TDC, $\psi[k] = \psi[k-1] + \alpha\cdot e[k]$, and β and α are the coefficients for the proportional and integral paths of the digital loop filter (DLF), T_{DCO} is the nominal DCO period and $t_{n,\text{DCO}}[h]$ is the random-walk DCO period jitter associated with the hth cycle. As the DPLL's stability requires that $\alpha \ll \beta$, the integral path of the DLF, $\psi[k]$ in (1), can be neglected without sacrificing the accuracy of the jitter transfer analysis. The TDC can be linearized with a linear gain, to whose output is added the TDC QE, as

$$e[k] = K_{\text{TDC}}\cdot\Delta t[k] + q_{\text{TDC}}[k], \quad (2)$$

where $\Delta t[k] = t_{\text{ref}}[k] - t_{\text{div}}[k]$ is the kth time difference between the timestamps of reference and divided signals.

Substituting (2) into (1) and some manipulations yield the difference equation (3), the sum in which contains $N_{\text{div}}[k]$ elements. Note that $N_{\text{div}}[k]$ produced by the DDSM divider controller can be expressed as $N_{\text{div}}[k] \equiv N + q_{\text{DDSM}}[k]$, where N is the non-integer nominal divider ratio and $q_{\text{DDSM}}[k]$ is the cycle-wise QE arising from the DDSM. Furthermore, as the reference clock jitter can be approximated by synchronous jitters associated with timestamps of the transition events [4], the term related to the reference in (3) becomes

$$t_{\text{ref}}[k+1] - t_{\text{ref}}[k] = T_{\text{ref}} + t_{\text{n,ref}}[k+1] - t_{\text{n,ref}}[k], \quad (4)$$

where T_{ref} and $t_{\text{n,ref}}[k]$ are the reference period and jitter.

Substituting (4) into (3), extracting the T_{DCO} term from the sum, and recalling that $T_{\text{ref}} = N\cdot T_{\text{DCO}}$ in the locked state, Eq. (3) can be simplified to

$$\Delta t[k+1] = (1 - K_{\text{TDC}}\beta K_T N)\cdot\Delta t[k] - q_{\text{DDSM}}[k]\cdot T_{\text{DCO}} + \text{“jitter terms contributed by intrinsic sources”}. \quad (5)$$

The right-hand side of (5) contains the jitter terms contributed by the TDC QE and reference and DCO jitters; these are quantitatively negligible compared to the $q_{\text{DDSM}}[k]\cdot T_{\text{DCO}}$ term, and hence can be omitted. Furthermore, simulation shows that the fractional-N operation suppresses the TDC gain by about 1000 times compared to the integer-N case [2], which pushes to zero the coefficient $K_{\text{TDC}}\beta K_T N$, which was optimized within (0,1) in the integer-N mode for loop stability. Therefore, in the steady state ($k \to \infty$), with the effect of the initial time difference $\Delta t[0]$ decaying to zero, (5) becomes

$$\Delta t[k+1] \approx -T_{\text{DCO}}\cdot\sum_{i=0}^{k} q_{\text{DDSM}}[i], \quad (6)$$

which indicates that the fractional-N input time difference is dominated by the waveform of the accumulated DDSM QE scaled by T_{DCO}.

Finally, taking the RMS values of both sides of (6) and substituting the standard deviation for the accumulated MASH DDSM QE [1] yields the fractional-N RMS input jitter as

$$\sigma_{\Delta t} \approx \begin{cases} \sqrt{\frac{1}{12}}\cdot T_{\text{DCO}}, & \text{for a first-order DDSM,} \\ \sqrt{\frac{1}{6}}\cdot T_{\text{DCO}}, & \text{for a MASH 1-1,} \\ \sqrt{\frac{1}{2}}\cdot T_{\text{DCO}}, & \text{for a MASH 1-1-1,} \\ \vdots & \end{cases}$$

The linearized gain and the variance of the QE of a generic N_b-bit TDC, taking as the input the accumulated QE of a MASH 1-1 or 1-1-1 DDSM, have been derived explicitly in [2], and these will be used directly in the linear analysis and PN predictions in the following sections.

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$$\Delta t[k+1] = \Delta t[k] + (t_{\text{ref}}[k+1] - t_{\text{ref}}[k]) - \sum_{h=N_{\text{div}}[k]\cdot k+1}^{N_{\text{div}}[k]\cdot(k+1)} \{K_{\text{TDC}}\beta K_T \cdot \Delta t[k] + \beta K_T \cdot q_{\text{TDC}}[k] + T_{\text{DCO}} + t_{n,\text{DCO}}[h]\}. \quad (3)$$

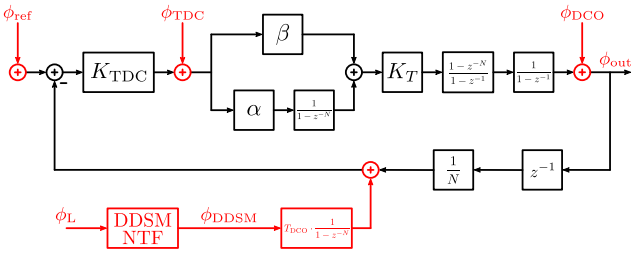

Fig. 3. LTI system model of a Fractional-N DPLL for the PN analysis. The injected noise/jitter sources are marked red.

III. Phase Noise Transfer Functions

The multi-rate system model shown in Fig. 2 can be linearized using a linear time-invariant (LTI) model, where $z = e^{j2\pi f/(N\cdot F_{\text{ref}})}$ [6]. The QE arising from the DDSM controller is injected into the feedback path as per the jitter transfer analyzed in Sec. II, as shown in Fig. 3. Note that the DDSM output QE, $q_{\text{DDSM}}[k]$, equals the QE injected into the final stage of the MASH, $q_{\text{L}}[k]$, that is Lth-order highpass filtered by the DDSM noise transfer function (NTF), where L is the order of the MASH DDSM.

For the conciseness of presentation, we represent the feed-forward (or open-loop) gain of the system as

$$G_{\text{FF}}(z) = K_{\text{TDC}} \cdot \left(\beta + \frac{\alpha}{1-z^{-N}}\right) \cdot K_T \cdot \frac{1-z^{-N}}{1-z^{-1}} \cdot \frac{1}{1-z^{-1}},$$

where K_{TDC} in the fractional-N mode is derived in [2], and the feedback gain as

$$G_{\text{FB}}(z) = \frac{1}{N} \cdot z^{-1}.$$

Hence, the loop gain of the system is

$$G_{\text{loop}}(z) = G_{\text{FF}}(z) \cdot G_{\text{FB}}(z). \quad (7)$$

1) $S_{\phi_{out}}$ due to Reference jitter: the system output PN power spectral density (PSD) due to the reference PN is

$$S_{\phi_{\text{out,ref}}}(f) = \left|\frac{G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot S_{\phi_{\text{ref}}}. \quad (8)$$

2) $S_{\phi_{out}}$ due to TDC QE: the system output PN PSD contributed by the TDC QE can be expressed as

$$S_{\phi_{\text{out,TDC}}}(f) = \left|\frac{1}{K_{\text{TDC}}} \cdot \frac{G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot S_{\phi_{\text{TDC}}}, \quad (9)$$

where $S_{\phi_{\text{TDC}}} = (2\pi F_{\text{ref}})^2 \cdot S_{Q_{\text{TDC}}}$ is the phase-domain PSD of the TDC QE transferred from the PSD of TDC QE, which is $S_{q_{\text{TDC}}} = \frac{\sigma^2_{Q_{\text{TDC}}}}{F_{\text{ref}}}$ as the TDC QE has a white power spectrum and its noise power is uniformly distributed in the bandwidth, F_{ref}. $\sigma^2_{Q_{\text{TDC}}}$ in the fractional-N mode is derived in [2].

3) $S_{\phi_{out}}$ due to DCO jitter: the PSD of the DCO-output-referred phase noise due to the DCO jitter is expressed as

$$S_{\phi_{\text{DCO}}}(f) = S_{\phi_{\text{DCO}}}(\Delta f) \cdot \left(\frac{2\pi(\Delta f)}{N \cdot F_{\text{ref}}}\right)^2 \cdot \frac{1}{|1-z^{-1}|^2},$$

where $S_{\phi_{\text{DCO}}}(\Delta f)$ is the PSD referred to the offset frequency Δf. The system output PN PSD due to the DCO jitter can be expressed as

$$S_{\phi_{\text{out,DCO}}}(f) = \left|\frac{1}{1+G_{\text{loop}}(z)}\right|^2 \cdot S_{\phi_{\text{DCO}}}(f). \quad (10)$$

4) $S_{\phi_{out}}$ due to DDSM QE: the PSD of the DDSM noise injected into the loop can be expressed as

$$T^2_{\text{DCO}} \cdot \left|\frac{1}{1-z^{-N}}\right|^2 \cdot S_{\phi_{\text{DDSM}}}(f)$$

where $S_{\phi_{\text{DDSM}}}(f) = \left|(1-z^{-N})^L\right|^2 \cdot S_{\phi_L}$ is the PSD as an output of the DDSM NTF. $S_{\phi_L} = (2\pi F_{\text{ref}})^2 \cdot S_{Q_L}$ represents the PSD of the QE injected into the Lth stage transferred to the phase domain, where $S_{Q_L} = \frac{\sigma^2_{Q_L}}{F_{\text{ref}}}$ as the QE is white and uniformly distributed in its bandwidth and $\sigma^2_{Q_L} = \frac{1}{12}$ is the variance of the QE produced by a 1-bit quantizer. Finally, the system output PN PSD due to the DDSM QE can be expressed as

$$S_{\phi_{\text{out,DDSM}}}(f) = \left|\frac{-G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot \left|\frac{T_{\text{DCO}}}{1-z^{-N}}\right|^2 \cdot S_{\phi_{\text{DDSM}}}(f). \quad (11)$$

The PSD of the DPLL's output PN is a linear combination of the PSD's contributed by each of the uncorrelated noise sources in (8)–(11), which is

$$S_{\phi_{\text{out}}}(f) = S_{\phi_{\text{out,ref}}}(f) + S_{\phi_{\text{out,TDC}}}(f) + S_{\phi_{\text{out,DCO}}}(f) + S_{\phi_{\text{out,DDSM}}}(f).$$

The above NTFs are used to predict the fractional-N DPLL's output PN in the next section, which is then compared with the behaviorally simulated counterpart.

IV. Verification Results

To verify the accuracy of our analysis, behavioral simulations using a multi-rate discrete-time model are performed, the PSDs of whose output PNs are extracted in Fig. 4 to check against the analytical predictions of Sec. III. The simulations use a BPD, 2-bit and 3-bit TDCs as the phase detector. For each of the cases, integer-N and fractional-N output PN performances are compared. The model parameters are those used in Sec. III of [6]. The reference frequency is 100 MHz. For the 2-bit and 3-bit TDCs, the time resolutions of 1.08 and 0.66 times the integer-N RMS input jitter are chosen, which minimizes the jitter for each case [5]. A MASH 1-1-1 divider controller is used to implement fractional-N operation; this sufficiently randomizes the spectrum of the TDC QE. The fractional nominal divide ratio is $N = 24 + 3277/2^{16}$.

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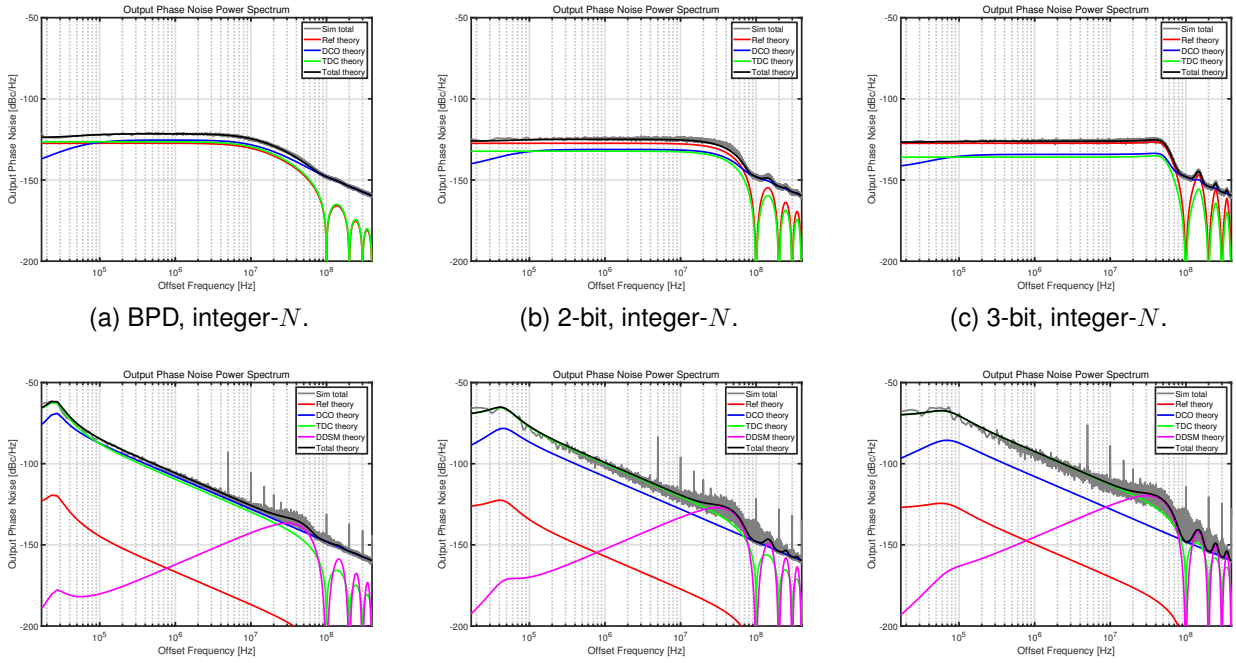

(a) BPD, integer-N. (b) 2-bit, integer-N. (c) 3-bit, integer-N.

(d) BPD, fractional-N. (e) 2-bit, fractional-N. (f) 3-bit, fractional-N.

Fig. 4. Simulated vs. predicted PN PSDs for DPLLs with a multi-bit TDC. MASH 1-1-1 divider controller is selected to facilitate the fractional-N operation. Sim total (gray) is the simulated output PN; Ref theory (red), DCO theory (blue), TDC theory (green), and DDSM theory (magenta) are the analytically predicted phase noises contributed by reference and DCO jitters, TDC and DDSM QE; Total theory (black) is the sum of all the predicted.

In each case, the prediction matches the simulation. Switching from the integer-N to the fractional-N mode, with the parameters of the loop and the intrinsic noise sources unchanged, the injected DDSM QE significantly degrades the K_{TDC}, which in turn reduces the unity-gain frequency f_u of (7). Note that f_u is the pole frequency of all the denominators of (8)–(11); reducing the value of K_{TDC} consequentially has the effect of reducing the loop bandwidth.

The reduced bandwidth does not change the close-in PN level contributed by the reference jitter, but effectively reduces the corner frequency of the lowpass filter. The DCO PN is highpass filtered; hence it contributes more noise due to the reduced bandwidth. The TDC's PN contribution is lowpass filtered. Its close-in PN level is determined by the power of the input-referred TDC QE, $S_{\phi_{\mathrm{TDC}}}/K_{\mathrm{TDC}}^2$. Switching to the fractional-N mode, the input-referred TDC QE is increased drastically as its value is mainly determined by the saturation of the top and bottom quantization levels overwhelmed by the much larger span of the TDC input jitter. The DDSM QE *per se* manifests some bumps in the output PN spectrum. Furthermore, DDSM-facilitated fractional-N operation exhibits spurs at integer and fractional multiples of the reference frequency.

V. Conclusion

In this paper, we address the PN-performance limits for a DPLL with a multi-bit TDC operating in the integer-N and fractional-N modes. The transfer mechanism of the input jitter is analyzed using a multi-rate discrete-time model, which reveals that the fractional-N input jitter is dominated by accumulated QE arising from the DDSM divider controller that is scaled by the nominal DCO period. Together with [2], this facilitates accurate linearized analysis of the TDC. We presented an LTI system model incorporating the DDSM noise injection and derived the PN transfer functions relating the noise/jitter sources to the system output. Our PN predictions are confirmed by behavioral simulations of DPLLs with BPD, 2-bit and 3-bit TDCs as examples.

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