

A 0.2–7.3-GHz Compact LNA with Super Linearity for 5G NR in 22-nm CMOS Technology

Kaiyun Deng^{*1}, Zan Zhou¹, Yingqi Liu¹, Haoyu Dong¹ and Haigang Feng^{*1}

¹ Shenzhen International Graduate School, Tsinghua University, Shenzhen 518055, China.

* Email: dkj23@mails.tsinghua.edu.cn, feng.haigang@sz.tsinghua.edu.cn

Abstract—This paper presents a broadband low-noise amplifier (LNA) with 6.7dBm third-order input intercept point (IIP3), 2.83 dB noise figure (NF) and 5.5mW power consumption. The LNA is suitable for 5G New Radio (NR) applications. To address the issue of low IIP3 caused by the reduced supply voltage in advanced processes, the derivative superposition (DS) technique is employed to enhance the IIP3. Simultaneously, the noise canceling (NC) method is applied to mitigate the trade-off between NF and wideband input impedance matching. The LNA is designed under the 22-nm CMOS process. Post-simulation results indicate that the proposed LNA achieves a peak gain of 13.3 dB and a -3dB bandwidth of 0.2-7.3 GHz. The FoM reaches 85.57 with die area of 0.0016 mm².

Keywords—CMOS LNA, broadband, current reuse, noise canceling, linearity improvement

I. INTRODUCTION

As the foundation of next-generation mobile systems, 5G wireless communication demands ultra-high capacity, data throughput, and spectral efficiency [1]. These requirements necessitate highly flexible and reconfigurable RF front-end architectures capable of supporting multiple frequency bands and communication standards. In this context, the design of broadband low-noise amplifiers (LNAs) has become a key enabler for software-defined radios (SDRs) and multiband receivers, which are essential for modern wireless platforms. 5G New Radio (NR), standardized by 3GPP, defines two frequency ranges, with Frequency Range 1 (FR1) extending the conventional sub-6 GHz spectrum up to 7125 MHz. This expanded frequency coverage imposes stringent requirements on the LNA in terms of bandwidth, gain flatness, noise figure, and linearity. Moreover, since the LNA directly influences the receiver's sensitivity and overall power consumption, its performance is critical to meeting 5G NR system-level specifications. As a result, broadband LNA design has attracted substantial attention in both academia and industry, as it plays a pivotal role in enabling scalable, power-efficient, and standard-compliant 5G receiver architectures.

Conventional approaches to extending the bandwidth of LNA typically rely on inductive peaking techniques, which require the integration of bulky passive inductors, leading to increased chip area and reduced design flexibility [2]–[7]. With the scaling of CMOS technologies, however, the intrinsic parasitic capacitance of MOS transistors has significantly decreased, enabling the realization of wideband LNAs without the need for inductors. This inductor-less design paradigm is particularly advantageous for broadband and multi-standard receivers, where compact area and integration are critical. Nonetheless, modern advanced processes also impose new challenges: the reduced supply voltage inherently limits the available voltage headroom,

which degrades the linearity of the LNA and consequently constrains the overall dynamic range of voltage-mode receiver front-ends. Previously reported LNAs in advanced processes have shown linearity below -2 dBm [3]–[5], [8]–[11], underscoring the need for new design strategies that can maintain both wideband operation and high linearity under low-voltage constraints. Moreover, noise cancellation (NC) techniques are widely adopted in broadband LNA designs to suppress the excessive noise contributed by the input matching transistors [3]–[5], [7]–[11].

In order to solve the problem of poor linearity of LNA under low power supply voltage in advanced processes, this paper designs a broadband LNA based on NC complementary pMOS-nMOS configurations. The LNA not only has excellent linearity in the entire 5G NR FR1, but also has a good trade-off in noise figure (NF), gain, and power consumption. The structure of this paper is organized as follows. Section II introduces the design of the proposed broadband LNA. Section III discusses the post-layout simulation results. Finally, section IV draws the conclusions.

II. PROPOSED BROADBAND LNA

The proposed LNA is shown in Fig. 1. Unlike the design in [4], which employs a voltage-shunt negative feedback resistor (R_F) to improve input matching and linearity, the R_F is intentionally removed in this work to eliminate the associated noise and stability concerns. The LNA covers overall 5G NR bands without inductors, with complementary pMOS-nMOS configurations in each stage to enhance linearity and reduce power consumption. In addition, the NC structure is applied to mitigate the trade-off between NF and wideband input impedance matching of the input common gate (CG) transistors. The common source (CS) NC stage includes an additional bias and is isolated by an ac coupling capacitor.

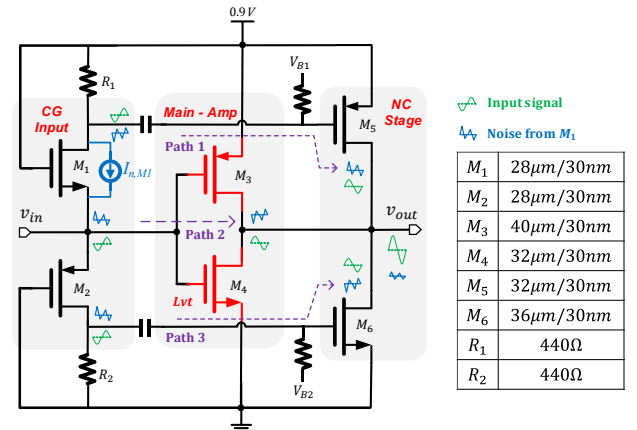


Fig. 1. Schematic of the proposed LNA.

A. Wideband Impedance Matching

With small parasitic capacitance in advanced processes, the LNA can achieve direct matching via the CG stage and load resistors R_1 and R_2 without voltage shunt negative feedback resistors, and high linearity can be further achieved using linearization techniques. The input impedance of this LNA is:

$$Z_{in} = \frac{R_1 + r_{o1}}{(1 + g_{m1} + g_{mb1})r_{o1}} // \frac{R_2 + r_{o2}}{(1 + g_{m2} + g_{mb2})r_{o2}} // \frac{1}{sC_X} \quad (1)$$

The output resistors r_{o1} , r_{o2} of M_1 , M_2 and the parasitic capacitance C_X at the input node play key roles in impedance matching. The input impedance matching remains stable throughout the entire 5G NR FR1 without using inductors, thanks to advanced processes with higher eigen-frequency f_T , and small C_X ensures good high-frequency matching. The LNA's output impedance, determined by four parallel drain impedances, offers flexibility for adjustment. For instance, [1] uses this design as a low-noise transconductance amplifiers in current-mode receivers, achieving higher output impedance and improved linearity by tuning $M_3 \sim M_6$. Therefore, through appropriate design, the proposed LNA supports impedance matching and efficient 50 Ω load driving without requiring an additional buffer stage. This not only simplifies the signal path and reduces power consumption, but also minimizes noise contribution and potential bandwidth limitations associated with conventional output buffers.

B. Analysis of Triple-Path Noise Canceling

Fig. 1 illustrates how the proposed LNA eliminates transistor channel thermal noise through three signal paths. Taking the thermal noise of M_1 as an example, the noise generates two opposite-phase voltages at its source and drain. Assuming the source noise is positive-phase and the drain noise is negative-phase, the thermal noise passes through Path 1 and produces positive-phase noise at the output. Meanwhile, the source noise of M_1 is processed by main amplifier and M_2 & M_6 auxiliary path, which produces negative-phase noise at the output. Unlike traditional CG noise cancellation, the thermal noise in Path 1 is canceled by Paths 2 and 3. The following discussion presents a calculation-based explanation. Consider only the thermal current noise generated by M_1 . According to the noise cancellation theory, the ratio of the resulting noise voltage at the source and drain of M_1 is given by

$$\frac{V_{n,D}}{V_{n,S}} = \frac{R_1}{R_S} \quad (2)$$

Let R_S be the impedance looking into the source of M_1 . If the transconductances of M_1 and M_2 are approximately equal, and their parallel combination matches the source impedance $1/R_S$, then the following condition holds:

$$\frac{V_{n,D}}{V_{n,S}} = \frac{R_1}{R_S} \approx \frac{R_1}{R_S // (1/g_{m1})} = 3g_{m1}R_1 \quad (3)$$

Without incorporating any auxiliary cancellation branches, and assuming the transconductances of M_3 and M_4 , as well as M_5 and M_6 , are equal respectively, the condition for noise cancellation becomes:

$$V_{n,D} \cdot g_{m5} = V_{n,S} \cdot 2g_{m3} \quad (4)$$

$$3g_{m1}R_1g_{m5} = 2g_{m3} \quad (5)$$

However, when auxiliary cancellation branches are introduced, and assuming $g_{m1}R_1 = g_{m2}R_2$, the new noise cancellation condition is given by:

$$3g_{m1}R_1g_{m5} = 2g_{m3} + g_{m2}R_2g_{m6} \quad (7)$$

$$2g_{m1}R_1g_{m5} = 2g_{m3} \quad (7)$$

By comparing equations (5) and (7), it is evident that the inclusion of auxiliary branches reduces the required g_{m3} by approximately 30%, which lowers the overall current consumption. This also allows for smaller device sizing in the common-source stage, resulting in improved impedance matching and enhanced high-frequency performance.

This reduces the current requirement of the main amplifier stage, lowering power consumption. Additionally, it reduces the size of the CG stage, improving high-frequency matching. The NC mechanism applies similarly to other transistors. On the other hand, the useful signals passing through these three paths are amplified with the same polarity and superimposed at the output. Fig. 2 shows the noise contribution of each component. It can be seen that the noise from M_1 and M_2 is only 0.46%, which is relatively small due to the high NC ratio of triple-path structure. And this is consistent with the above analysis.

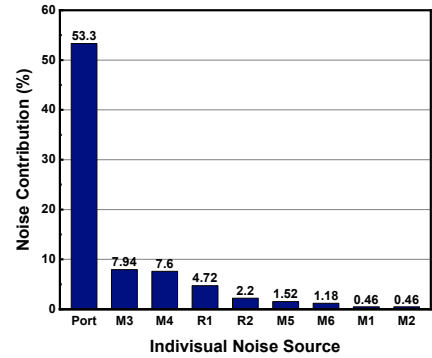


Fig. 2. Simulated relative noise contributions at 2 GHz.

C. Derivative superposition Linearization

Operating under a low supply voltage of 0.9 V inherently limits the voltage headroom and makes achieving high linearity particularly challenging. To mitigate this limitation, the proposed LNA adopts the derivative superposition (DS) technique, which effectively suppresses nonlinearity by engineering the transconductance (g_m) characteristics of the input stage [12]. Specifically, as demonstrated in [3] and [4], this technique utilizes carefully biased complementary pMOS–nMOS transistor pairs to cancel the first- and second-order derivatives of the transconductance, thereby minimizing third-order intermodulation distortion. In the proposed design, optimized biasing ensures that the nonlinear components of the overall transconductance curve are suppressed around the operating point, significantly improving linearity without incurring additional power or area overhead. This makes the DS method particularly well-suited for low-voltage broadband LNAs targeting modern wireless systems where both linearity and power efficiency are critical. The input CG transistors M_1 and M_2 generate nonlinear currents, but their gain is low, contributing mainly to g_m for input matching rather than linearity. In contrast, the complementary output pair M_5 and M_6 dominate the LNA's linearity. Their transconductance and nonlinear components, modeled as a nonlinear current source

using Volterra series expansion, determine the total output current. Considering third-order nonlinear distortions, the total output current of the M_5 & M_6 pairs is equal to

$$i_{total} = i_{dsN} + i_{dsP} \\ = (g_{m6} + g_{m5})v_{gs} + (g'_{m6} - g'_{m5})v_{gs}^2 + (g''_{m6} + g''_{m5})v_{gs}^3 \quad (7)$$

It is obvious that the total transconductance (g_{m56}), subtraction of first-order (g'_{m56}), and sum of second-order derivatives (g''_{m56}) determine the output current and linearity through DS. Since the ac input signal for NMOS/PMOS are out of phase, g_{m56} increases in the triple-path NC structure, while g'_{m56} and g''_{m56} decrease at optimal bias. Fig. 3 shows g'_{m56} and g''_{m56} varying with gate bias voltage ($V_{B1} = V_{B2} = V_B$). At specific bias points, g'_{m56} and g''_{m56} drop to nearly zero. This demonstrates effective cancellation of second- and third-order nonlinear currents, aligning with theoretical analysis. By reducing nonlinear currents mixed with inputs via C_{gd} feedback, both second-order input intercept point (IIP2) and third-order input intercept point (IIP3) can significantly improve, with IIP3 peaking at the optimal bias. Consequently, this DS technique solves LNA linearity challenges under advanced processes, enabling high linearity at a low supply voltage.

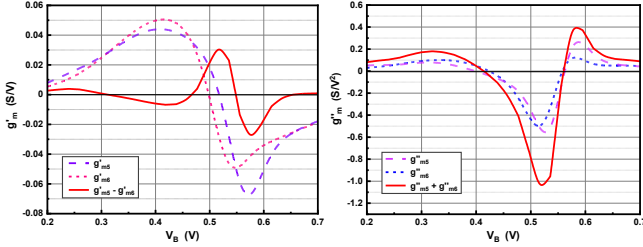


Fig. 3. (a) First-order derivatives of the g_m of the output NC stage. (b) Second-order derivatives of the g_m of the output NC stage.

III. POST-LAYOUT SIMULATION RESULT

The proposed LNA is implemented using 22-nm CMOS technology. All design parameters are shown in Fig. 1. The parasitic capacitance of 100 fF on pads and the inductance of 0.8 nH on the bonding wires are considered. The layout of the proposed LNA is shown in Fig. 4, with a core area of $40 \mu\text{m} \times 40 \mu\text{m}$. By carefully designing the MOS transistor of output stage, it does not require an additional buffer to drive the output load, which is beneficial for the power consumption, gain, and NF of the entire circuit.

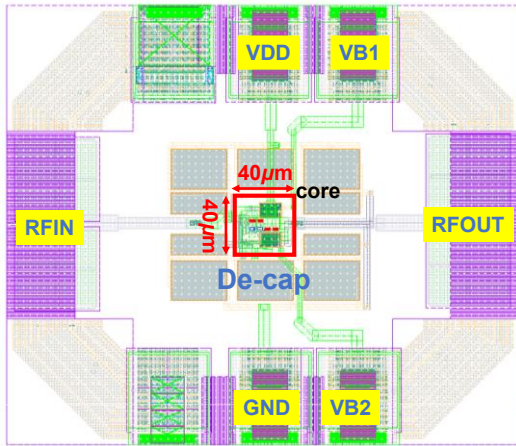


Fig. 4. Layout of the proposed LNA.

A. Monte-Carlo Simulation Results

Process variations and device mismatches can significantly degrade the effectiveness of noise-cancellation techniques by disrupting the precise conditions required for constructive signal summation and destructive noise suppression. To quantitatively evaluate their impact on the noise performance, extensive Monte Carlo simulations were conducted under two scenarios: mismatch-only and full process variation. As shown in Fig. 5, at 1 GHz, the standard deviation of the NF is 0.005 dB due to device mismatch and 0.0854 dB under full process variation. At 7 GHz, the standard deviation increases slightly to 0.0102 dB and 0.0944 dB, respectively. These results demonstrate that while mismatch introduces only minor variation, process fluctuations have a more pronounced effect, particularly at higher frequencies. Nevertheless, the overall NF variation remains within a narrow range, indicating that the proposed architecture maintains strong robustness against both mismatch and process-induced deviations, making it well-suited for wideband and process-tolerant RF applications.

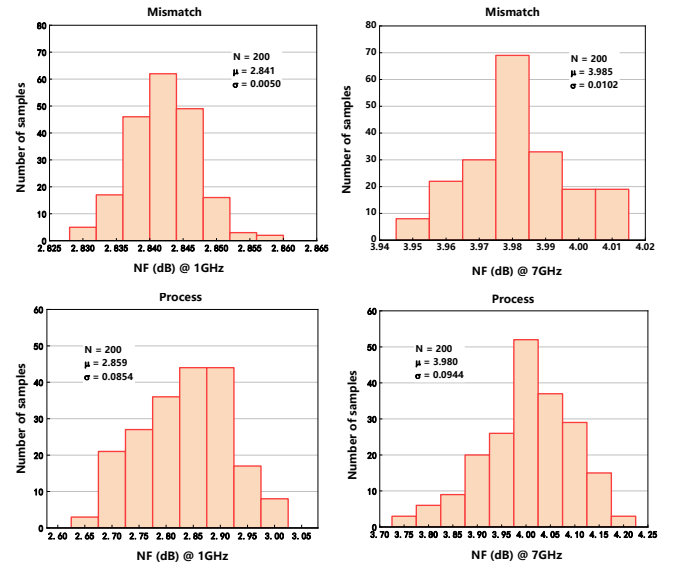


Fig. 5. Monte Carlo simulation results for NF.

B. S-parameter, NF and Linearity Simulation Results

Fig. 6 presents the simulation results of the S-parameter analysis and NF. IIP3 at 5.5 GHz and the entire frequency band are shown in Fig. 7. P1dB at 7 GHz and the entire frequency band are shown in Fig. 8. The proposed LNA matches well in the 0.2-7.3 GHz, covering the entire bandwidth of 5G NR FR1. Within the 3-dB bandwidth, the peak gain is 13.3 dB and the minimum NF is 2.83 dB. The IIP3 of LNA is obtained through a two-tone test, reaching up to 6.7 dBm across the entire operating range. The proposed LNA operates at a low supply voltage of 0.9 V, with a total static current of 6.1 mA and a total power consumption of only 5.5 mW. Table I benchmarks the performance with previously published broadband LNAs. Compared to previous designs, the proposed LNA demonstrates excellent linearity at a low supply. Although the LNA in [4] also achieves IIP3 of 5.8 dBm, it operates at a power supply voltage of 1.6V. In contrast, the proposed LNA offers a good trade-off across other performance metrics, with its FoM reaching a very high level. This makes it a viable solution for overcoming the linearity limitations of LNAs in receiver at a low supply using advanced processes.

TABLE I
SUMMARY OF TYPOGRAPHICAL SETTINGS

Ref.	CMOS Tech.	BW (GHz)	Gain (dB)	NF _{min} (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	Num. of inductors	Area (mm ²)	FoM ₁	FoM ₂
This Work*	22 nm	0.2-7.3	13.3	2.83	6.7	0.9	5.5	0	0.0016	29.65	85.57
[4] TMTT'20	65 nm	1-20	12.8	3.3	5.8	1.6	20.3	3	0.096	22.70	43.06
[5] JSSC'21	28 nm	0.02-4.5	15.2	2.09	-4.63	1	4.5	1	0.03	10.08	40.54
[6] TMTT'21	40 nm	1-11	17	3.5	-2.8	1.2	9	2	0.061	10.46	34.75
[9] ASICON'23*	40 nm	0.3-4.3	21.7	3.2	-12.4**	1.1	3.6	0	NR	2.53	/
[10] TCAS I'24	28 nm	0.2-2.85	20	2.9	-12.3	0.6	1.74	0	0.0048	-0.5	45.88

*Post-layout simulated results **calculate from IIP3=P1dB+9.6dB NR: Not report

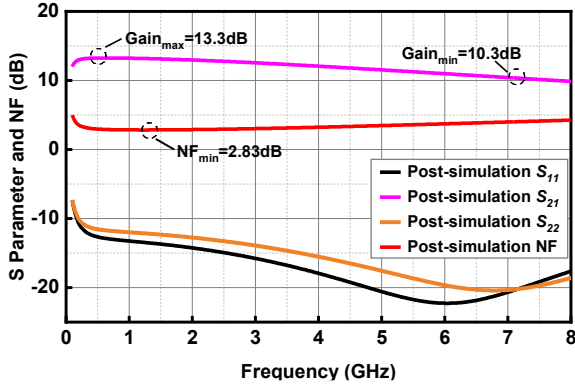


Fig. 6. Post-layout simulated results of S-parameter and NF.

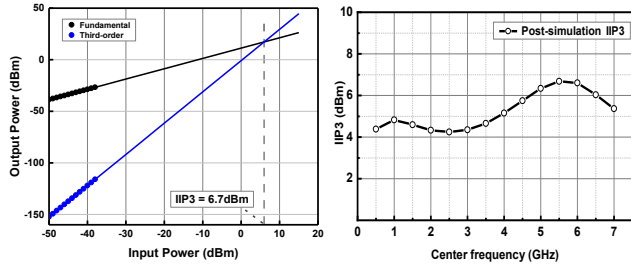


Fig. 7. Post-layout simulated results of IIP3. (a) IIP3 at 5.5 GHz. (b) IIP3 of the whole band.

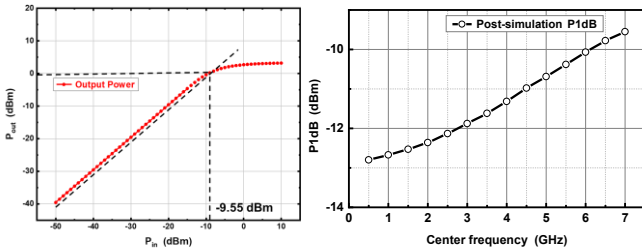


Fig. 8. Post-layout simulated results of P1dB. (a) P1dB at 7 GHz. (b) P1dB of the whole band.

$$FoM_1 = 20 \log_{10} \left(\frac{BW [GHz] \cdot Gain [abs] \cdot IIP_3 [mW]}{P_{DC} [mW] \cdot (F_{min} - 1)} \right) \quad (8)$$

$$FoM_2 = 20 \log_{10} \left(\frac{BW [GHz] \cdot Gain [abs] \cdot IIP_3 [mW]}{P_{DC} [mW] \cdot (F_{min} - 1) \cdot A [mm^2]} \right) \quad (9)$$

IV. CONCLUSION

This paper presents a broadband LNA topology to solve the problem of poor linearity caused by low supply voltage in

advanced processes for 5G NR applications. A novel derivative superposition technique is utilized to enhance IIP3. The proposed LNA features a compact design with extremely small area and covers the full 5G NR bandwidth without inductors, which is well-suited for high-linearity MIMO 5G mobile communication receivers.

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