18.1 A 600Gb/s DP-QAM64 Coherent Optical Transceiver Frontend with 4x105GS/s 8b ADC/DAC in 16nm CMOS

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An ADC/DAC-based coherent optical transceiver [1] is a promising technique to boost the throughput of metro/long-haul links beyond 600Gb/s/λ. It leverages the powerful digital signal processors (DSP) in scaled CMOS processes to enable high-spectral-efficiency modulation formats such as dual-polarization quadrature-amplitude modulation (DP-QAM). At the DSP interface, it uses four well-synchronized DACs and ADCs to generate and capture the four streams of analog signals that are carried by the same light in DP-QAM format (Fig. 18.1.1). In 600Gb/s links that use DP-QAM64 and feedforward error correction (FEC) coding, the baud rate can go up to 70GBaud/s. This requires an ADC/DAC bandwidth of 40GHz and a sampling rate of 105GS/s to satisfy the oversampling ratio needed for spectrum shaping and clock-data recovery. Meanwhile, the ADC/DAC have to achieve low noise and high linearity to achieve the SNDR needed for DP-QAM64 at low power consumption. In this paper, we present a 600Gb/s/λ DP-QAM64 coherent optical transceiver frontend that fully integrates a 4-way 78~105GS/s 8b ADC/DAC in a DSP chip in 16nm CMOS. It supports flexible rates of 100, 200, 300, 400, 500, 600Gb/s by DP-QPSK and DP-QAM8/16/32/64 with a variable baud rate for long-haul, metro, and ZR applications.

The receiver includes four 105GS/s ADCs that share one PLL. As shown in Fig. 18.1.2, each receiver ADC has a Π-shape network of tunable resistors at its input, which provides constant 50Ω termination and variable attenuation so that the following circuits are not saturated by a large input signal. It is followed by a highly-linear broadband VGA that drives the large loading circuits and rejects the common mode ripple at the input. To achieve high linearity, a distortion cancellation technique is employed, where a cancellation pair is used in parallel with the main differential pair but with their outputs connected in opposite polarity. The cancellation pair is designed to have low gain but high distortion, so that it cancels the distortion of the main pair without reducing the total gain and bandwidth significantly. This cancellation is insensitive to PVT variations, in that it only depends on the ratios of device sizes and bias currents. The VGA uses peaking inductors at its input and output to extend bandwidth up to 40GHz. The integration of a VGA makes the system more versatile and scalable.

Each 105GS/s ADC has 192 asynchronous successive-approximation-register (SAR) ADCs that are time-interleaved by a two-stage track-and-hold (T/H) circuit. The 1st-stage T/H has four super source followers (SSF) [2] in parallel, and each SSF drives four high-speed samplers that have non-overlapping tracking windows; the 2nd-stage T/H consists of sixteen voltage buffers, and each drives twelve SARs that take turns to take in the sampled data when the corresponding 1st-stage sampler is in hold mode. This two-stage structure reduces the number of critical clocks to sixteen 1st-stage sampling clocks, which are placed evenly in time by a skew calibration circuit. It also enhances bandwidth matching between interleaved signal paths by confining the high-frequency signal to the 1st-stage T/H that uses symmetric routings and has well-controlled surroundings. We use the SSF to drive the large loading in the T/H, in that its feedback loop generates complex poles that extend signal bandwidth and make settling faster. It is biased by a constant-gm current, so that its poles are less sensitive to PVT variation. The sampling switches use neutralization capacitors between their inputs and outputs in order to reduce signal feedthrough in hold mode. The asynchronous SAR outputs are synchronized by a two-level retimer and sent to the DSP in parallel. The interleaving mismatches in gain, offset and clock skew are calibrated by analog and digital loops that are fully integrated on chip.

The four ADCs, each having numerous finite states machines (FSM) in their dividers, tokens and SARs, must be synchronized so that the time-interleaved SAR output data is in the right order for the DSP. The sampling clocks of the four ADCs must be aligned to ps accuracy to capture the phase information in the DP-QAM signal. We use a two-step reset scheme along with a low-skew global clock distribution circuit to achieve the goal. During startup (Fig. 18.1.1), RST_ADC is asserted at the four ADCs to reset all FSMs to a pre-defined state, and RST_CLK is asserted at the PLL to reset the quadrature clock buffers shared by the four ADCs to a desired initial state. Then, RST_ADC is released first so that ADCs get ready to function; RST_CLK is released after a short delay so that the quadrature clock and thus the FSMs in the ADC start to toggle from a known state. As RST_CLK is used to gate the high-speed quadrature clocks that have <10ps edge spacing, RST_CLK is carefully retimed to rule out any metastability and glitch in the clocks when it is released. The global clock distribution circuit uses a tree structure that is symmetric from PLL to the four ADCs. In order to reduce jitter and random skew, it uses only two stages of CMOS buffers, each of which is large in size and drives a long clock channel of 1.2mm. The transmission line effect of the clock channel is carefully modeled to make sure the ADC clock has low jitter and low skew with sharp rail-to-rail edges.

The transmitter consists of four 8b DACs operating at 105GS/s and one shared PLL. As shown in Fig. 18.1.3, the DAC employs a current steering structure that utilizes quarter-rate clock and half-rate data at its input to achieve high sample rate and bandwidth at low power. It also uses a 3b-thermometer and 5b-binary segmentation in which the bits are spatially scrambled in layout to average out systematic errors and improve ENOB. Each DAC bit consists of two pulses from DAC-I and DAC-Q. The beginning edge of one pulse is triggered by the clock, while that of the other pulse is triggered by the half-rate input data transition, as are the ending edges of the two pulses. In this way, every bit transition is a combination of two edges that are triggered by clock and data respectively, and all bits are systematically matched. Compared to half-rate design, the presented architecture avoids the half-rate clock that has a tiny pulse width of <10ps, and thus is more power efficient and more scalable for high-speed applications. Compared to a conventional quarter-rate design, which has three data switches in idle while only one is active at a time, the presented design has only half of the switches in idle and thus a smaller loading capacitor at the output net. This helps achieve larger bandwidth.

In this DAC architecture, two quarter-rate clock edges should ideally be placed at the center of the half-rate data eye, while the other two are used to generate the half-rate data in the 4:2 MUX. This clock/data alignment is realized by a clock path that mimics the 4:2 MUX and pre-driver in the data path. A slight misalignment between clock and data would not affect performance, since the two pulses from DAC-I and DAC-Q would skew in opposite directions and cancel their effect. On the other hand, the quadrature clock phases and duty cycles must be calibrated to high accuracy to minimize the interleaving tones at |Fout±Fs/4| and |Fout±Fs/2|. Considering that the edges in the half-rate data directly pass to the DAC output, the 4:2 mux and pre-driver need to deliver clean data transitions (<1ps ISI) at the DAC input. To this end, the pre-driver uses regulated power rails so that its output maintains sharp edges and optimal voltage levels to toggle the DAC's differential pairs. The reduced voltage swing avoids driving the DAC transistors to unnecessarily high or low voltages and improves operation speed and linearity.

The RX and TX share the same charge-pump-based PLL architecture in Fig. 18.1.1. Two low-noise LC VCOs, which use stacked metals to realize high-Q inductors, are employed to cover 39~46GHz and 46~53GHz, respectively. They are followed by a CML MUX and a divide-by-2, which generates the low-skew quadrature clock phases that drive the ADCs and DACs. The charge pump and loop filter are fully differential for better noise immunity. Great effort was made to reduce interference between different blocks by proper floor planning and by supply network optimization. These are critical for generating the low-jitter clock that samples high-frequency signals.

The design is fully integrated in a DSP chip in standard 16nm CMOS that demonstrated 600Gb/s/λ transport in DP-QAM64 format and has been in mass deployment. In analog measurement, the ADC achieves SNDR and SFDR of 42.8dB and 60.5dB at 0.51GHz, as well as 39.2dB and 50.7dB at 20.9GHz, and -3dB bandwidth of 40GHz (Fig. 18.1.4). The DAC achieves THD of >6b up to 27.5GHz, and -3dB bandwidth of 35GHz (Fig. 18.1.5). The PLL jitter measured through the TX DAC is 51fs integrated from 10kHz to 100MHz, and the two VCOs cover 39~53GHz with margin. The four transceiver lanes are well synchronized, with static skew of <2ps and voltage-temperature drift of <0.5ps in measurements that include the package and board. The total area of the receiver and transmitter are 5.5mm² and 2.7mm², respectively (Fig. 18.1.7). In summary, the design achieves better SNDR and SFDR in the ADC and DAC and lower clock jitter in the PLL than prior arts, which enables 50% higher spectral efficiency by higher-order modulation of DP-QAM64. The ADC also achieves a record Schreier FOM of 148.0dB, although it is in an older process and integrates more analog functions in the front end (Fig. 18.1.6).

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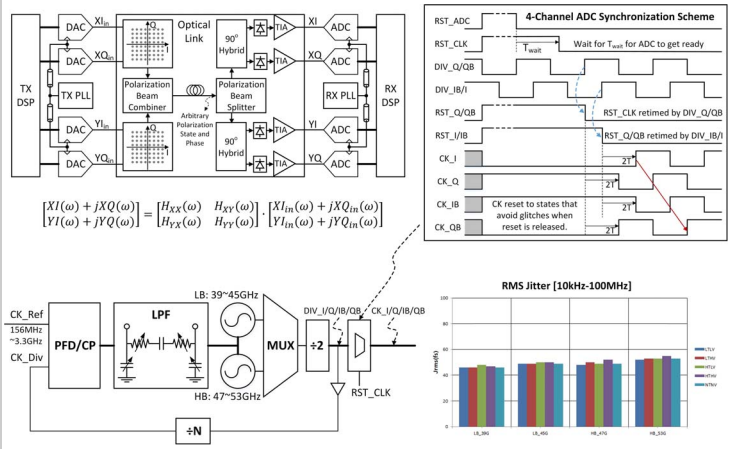


Figure 18.1.1: Transceiver top-level diagram, PLL with synchronization scheme, and PLL jitter measurement.

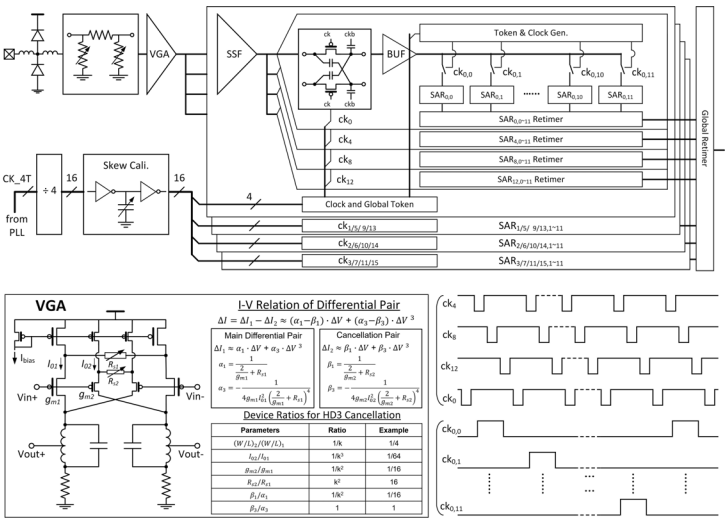


Figure 18.1.2: RX top-level structure with critical circuits and 2-stage T/H timing diagrams.

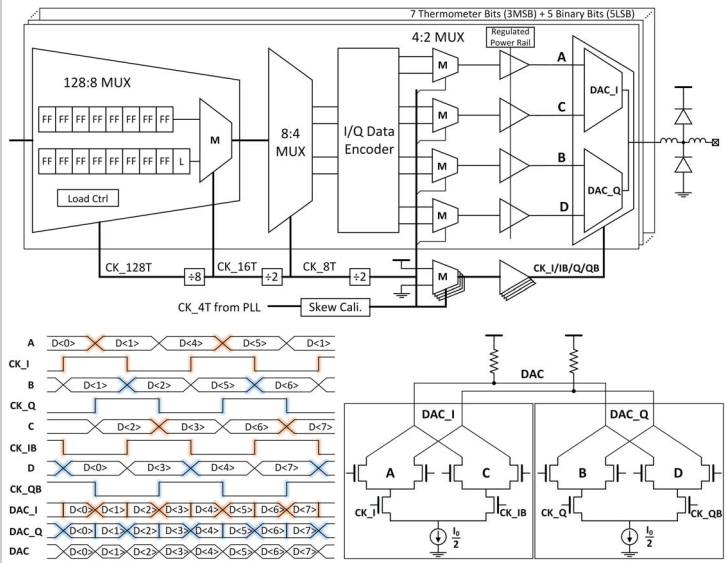


Figure 18.1.3: TX top-level structure and DAC timing diagram.

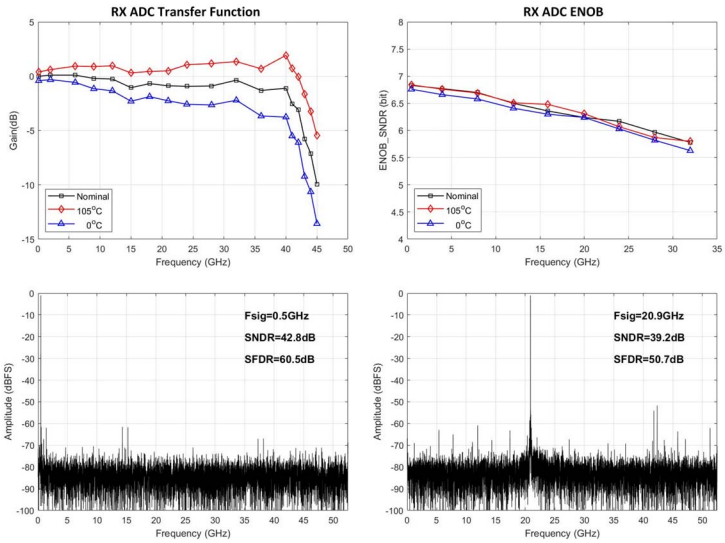


Figure 18.1.4: RX ADC measurement at 105GS/s: transfer function, ENOB, and spectrums at low and high frequencies.

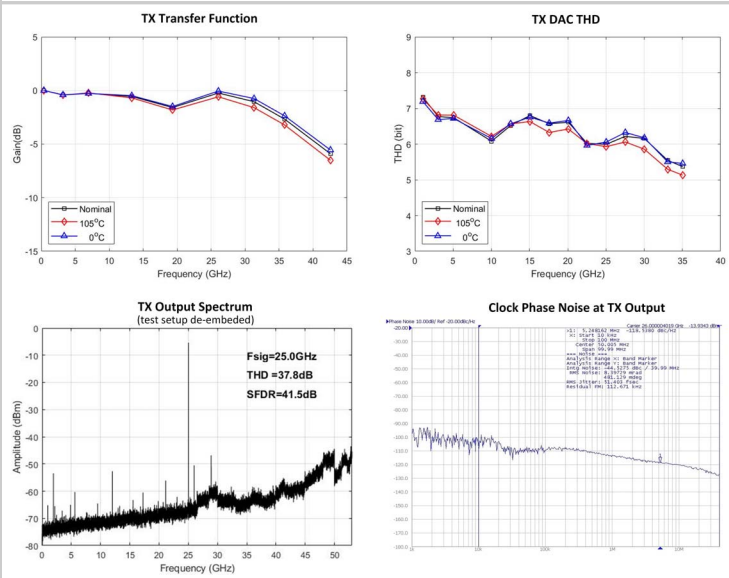


Figure 18.1.5: TX DAC measurement at 105GS/s: transfer function, THD, spectrum and clock jitter spectrum.

	ISSCC14 [3]	ISSCC17 [4]	ISSCC18 [5]	ISSCC21 [6]	This Work*
Process	32nm SOI	20nm CMOS	14nm CMOS	7nm CMOS	16nm CMOS
Application	--	100Gbps DP-QPSK	--	400Gbps DP-QAM16	600Gbps DP-QAM64
Sample Rate (GSps)	70~100	4x(55~69)	24~72	4x(40~97)	4x(78~105)
BW (GHz)	22	19	21	TX:35, RX:40	TX:35, RX:40
Resolution (bit)	8	8	8	8	8
ADC					
SNDR (dB)	36.0@0.2G 33.0@19.9G (tested at 90GS/s)	39.7@0.2G 32.5@19G	39.3@0.2G 34.2@20G	41.1@0.12G 35.1@19.4G	42.8@0.51G 41.1@13.0G 39.2@20.9G
SFDR (dB)	41.4@19.9G	43@8G	44.1@36.1G	44.0@0.12G 42.4@19.4G	60.5@0.51G 52.8@13.0G 50.7@20.9G
Power(mW)	ADC: 667 (no VGA)	ADC: 950 (VGA included)	ADC: 235 (no VGA)	ADC: 311 (no VGA)	ADC: 698 VGA: 62
$FOM_{S,hf}$(dB)**	141.3@19.9G	138.1@19G	146.1@20G	147.0@19.4G	148.0@20.9G
DAC					
Output Swing (mV)	--	700	--	1100	1200
THD (dB)	--	43.9@1G 37.8@14.7G	--	45.1@0.1G 39.8@3G 35.0@23G	45.5@1G 41.9@3G 37.8@25G
Power(mW)	--	620	--	307	344
PLL					
RMS Jitter (fs)	--	79	--	150	51

* ADC and DAC results are measured at 105GSps.

**$FOM_{S,hf}$ = SNDR+10log10(Fs/2/Power).

Figure 18.1.6: Table of comparison.

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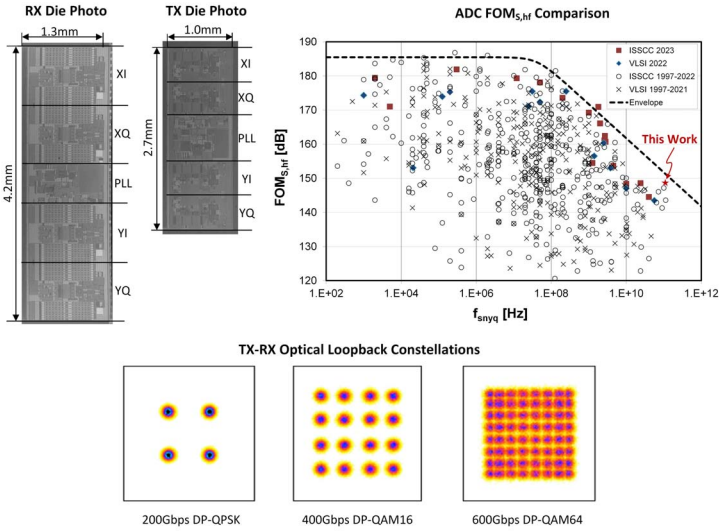


Figure 18.1.7: Die photos, ADC FoM comparison and TX-RX optical loopback constellations.

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