

An X-Band Filtering-Limiter Low Noise Amplifier in 180 nm CMOS Technology

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Abstract—In this paper, a filtering-limiter low-noise amplifier (LNA) based on 180 nm CMOS technology is proposed. The limiter utilizes an absorptive structure composed of two limiter units to enhance power handling capability, achieving a power capacity of 40 dBm, and introduces a transmission zero by incorporating an LC series branch, achieving an insertion loss (IL) of 1.5 dB at 10 GHz, and providing approximately 20 dB of stopband suppression for frequencies greater than 19 GHz. The LNA utilizes a common-source (CS) and cascode structures to achieve a peak gain of 17.5 dB and a minimum noise figure (NF) of 2.8 dB. The filtering-limiter LNA achieves a gain of 16 dB at 10 GHz, with an NF ranging from 4.5 to 5 dB over the 8–12 GHz, it consumes 24 mW and the core circuit area is 0.55 mm².

I. INTRODUCTION

With the rapid development of wireless communication technology, the demand for radio frequency (RF) integrated circuits is growing. In the RF front-end module, the low-noise amplifier (LNA), as a key component, is responsible for amplifying the received signals but is susceptible to damage from high-power input signals, such as blocking signals or transmitter leakage. A limiter is required to protect against high-power interference while maintaining minimal insertion loss (IL) to preserve the LNA's noise figure (NF) and receiver sensitivity [1]. Integrating the limiter with the LNA can reduce losses and chip area. However, traditional limiters lack frequency selectivity, potentially amplifying out-of-band interference and harmonic components, which degrades receiver performance. Therefore, studying limiters with filtering characteristics is import. A filtering-limiter not only protects sensitive components but also effectively suppresses out-of-band interference. It's necessary to ensure that the passband IL remains low to minimize impact on the NF.

Currently, limiter-LNAs aim to achieve high power capacity, high gain, and low NF, most designs use GaAs technology [2–4], which can achieve a power capacity greater than 35 dBm, an NF less than 2.6 dB. Integrating a filtering structure into the limiter [5] improves the ability to suppress out-of-band interference signals. Despite the superior performance achieved by circuits using GaAs technology, they have larger areas, higher power consumption, and higher circuit costs. In contrast, CMOS technology offers high integration density and lower costs, providing significant advantages for fully integrated RF front-end systems.

Based on 180 nm CMOS technology, this paper presents the design of an X-band filtering-limiter LNA, achieved by

cascading a filtering-limiter with an LNA. This design features low power consumption and a small chip area while maintaining high power capacity. Detailed design aspects of the filtering-limiter and LNA are discussed in Section II, with the circuit layout and simulation results presented in Section III.

II. CIRCUIT DESIGN

A. Structure of filtering-limiter LNA

Fig. 1 shows the complete schematic of the filtering-limiter LNA, formed by directly cascading the filtering-limiter section with the LNA section. The filtering-limiter restricts the input high-power signal to protect the downstream circuit. The LNA is responsible for amplifying the signal and suppressing noise in subsequent stages.

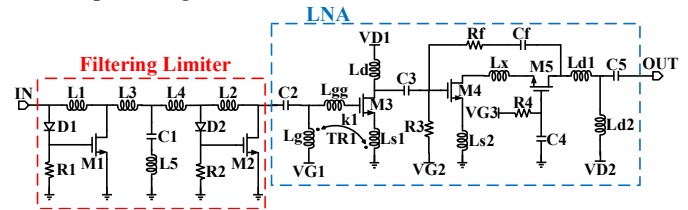


Figure 1. Schematic of the filtering-limiter LNA.

The design of these two sections is further analyzed as below.

B. Design of filtering-limiter

limiters can generally be divided into reflective and absorptive types. Reflective limiters often use an anti-parallel diode structure, reflecting most of the input power back to the input port, which provides high power handling capability. However, under limiting conditions, the standing wave ratio (SWR) deteriorates, limiting the application of reflective limiters [6]. As shown in Fig. 1, the filtering-limiter adopts an absorptive structure with two limiter units and an LC series branch. The limiter unit, depicted in Fig. 2(a), comprises a schottky diode and a MOSFET switch, the schottky diode has dimensions of $W = 4 \mu\text{m}$, $L = 2 \mu\text{m}$, and finger = 1. When a low-power signal is input, the diode outputs a very small voltage, and the switch remains off, making the limiter a direct pass circuit with minimal path loss. However, when a high-power signal is input, the diode outputs a sufficiently large voltage to turn on the transistor, diverting part of the power to the ground and limiting the power output to the next stage to a safe value [7]. Adding a series branch with $L5 = 400 \text{ pH}$ and $C1 = 175 \text{ fF}$ to the limiter units introduces a transmission zero near 19 GHz, attenuating signals above this frequency by 20 dB.

The MOSFET as a switch equivalent model is shown in Fig. 2(b). When the gate-source voltage (V_{GS}) of the transistor is less than the threshold voltage (V_{TH}), the transistor is equivalent to being in the off state. In this case, the equivalent circuit is represented as STATE:OFF in Fig. 2(b). When V_{GS} is greater than V_{TH} , the transistor is equivalent to being in the on state. In this case, the equivalent circuit is represented as STATE:ON in Fig. 2(b).

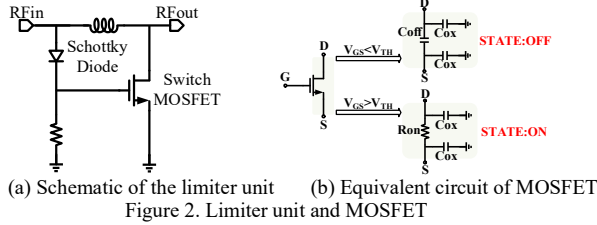


Figure 2. Limiter unit and MOSFET

The simulation results of the filtering-limiter are shown in Fig. 3. As illustrated in Fig. 3(a), the input and output reflection coefficient (S_{11} , S_{22}) are both less than -10 dB within 8-12 GHz, with an IL of 1.5 dB at 10 GHz and a stopband suppression of 20 dB for frequencies greater than 19 GHz. Fig. 3(b) shows that the limiting threshold of the limiter is 10 dBm, the flat leakage level is about 10 dBm, and the power handling capacity is 40 dBm.

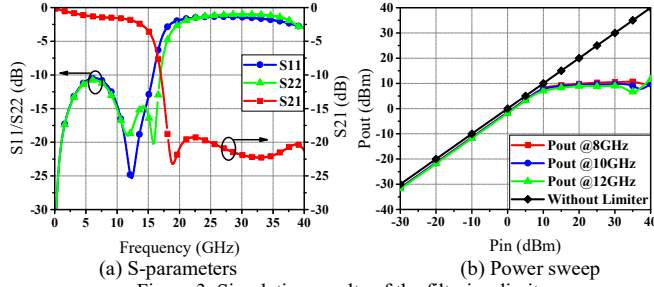


Figure 3. Simulation results of the filtering-limiter

C. Design of LNA

The LNA employs common-source (CS) and cascode structures, as shown in Fig. 1. The first-stage CS utilize source degeneration inductor L_{s1} to better balance noise and gain in input matching while also improving stability. The input matching network uses a feedback structure based on a shunt-series transformer to achieve broadband impedance matching. The gate series inductor L_{gg} is also used to adjust the gain frequency response of the CS stage. The second-stage cascode utilize source degeneration inductor L_{s2} , serving the same purpose as in the CS stage. In addition, an inductor L_x is added at the junction of the CS and common-gate (CG) in cascode stage to resonate out the parasitic capacitor, thereby increasing the high-frequency gain of the circuit. Moreover, the feedback network comprising R_f and C_f enhances the stability of the cascode stage while suppressing low-frequency gain to achieve a flatter gain response. Furthermore, for the output stage, a series peaking inductor L_{d1} and a shunt peaking inductor L_{d2} are employed to extend the 3 dB bandwidth.

Fig. 4 shows the input matching performance of the CS stage with the shunt-series transformer TR1. The real and imaginary parts of the input impedance (Z_{in})

and $\text{Im}[Z_{in}]$. The Z_{in} is close to 50Ω in the 8-12 GHz frequency range, with S_{11} reaching its minimum around 10 GHz, indicating good input matching. Fig. 5 illustrates the 3D structure of the shunt-series transformer TR1, with parameters $L_g = 1.34$ nH, $L_{s1} = 410$ pH, and $k_1 = 0.38$. Both coils are using M6 layer metal to enhance their quality factor (Q).

As shown in Fig. 6, there exists a significant parasitic capacitor between CS and CG in the cascode stage. This parasitic capacitor includes the drain-to-substrate capacitor C_{db4} of CS, the source-to-substrate capacitor C_{sb5} and the gate-to-source capacitor C_{gs5} of CG [8]. These parasitic capacitors can reduce the high-frequency gain of the circuit. Therefore, introducing L_x to resonate with the parasitic capacitor helps increase the gain at high frequency, thereby reducing the transistor's noise contribution.

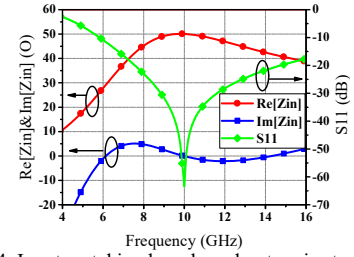


Figure 4. Input matching based on shunt-series transformer

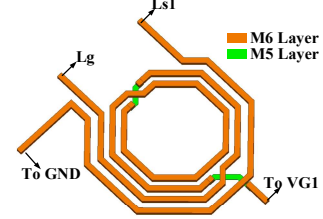


Figure 5. Shunt-series transformer

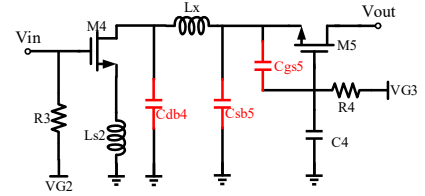


Figure 6. The inductor L_x resonate with the parasitic capacitor

Fig. 7 shows the simulation results of the LNA, demonstrating a small signal gain (S_{21}) of $16.8 \text{ dB} \pm 0.7 \text{ dB}$ within the 8-12 GHz frequency range, with a peak gain of 17.5 dB at 10 GHz. It has a 3 dB bandwidth of 7-13.3 GHz and an NF of 2.8-3.2 dB. Additionally, S_{11} and S_{22} are both less than -8 dB within 8-12 GHz.

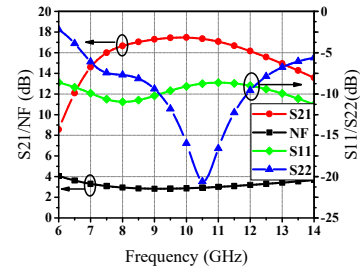


Figure 7. Simulated S-parameters and NF of the LNA

III. SIMULATION RESULTS

The layout of the filtering-limiter LNA is shown in Fig. 8. The layout area occupies 0.79 mm², including the RF PADs and DC PADs, and the core area is 0.55 mm². The circuit draws 4.7 mA from VD1 at 1.8 V and 5.7 mA from VD2 at 2.7 V, with an approximate power consumption of 24 mW.

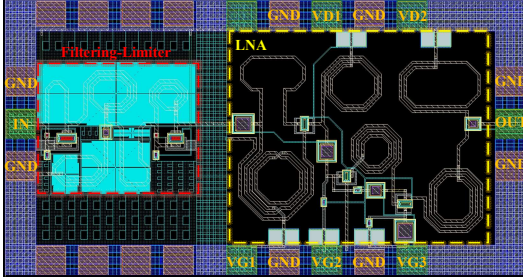


Figure 8. Layout of the filtering-limiter LNA

Fig. 9 shows the simulation results of the filtering-limiter LNA. The small signal gain (S21) is 15.3 ± 0.7 dB within the 8-12 GHz range, with a peak value of 16 dB at 10 GHz. The NF ranges from 4.5 to 5 dB, S11 is less than -7 dB, and S22 is less than -8 dB. The minimum stability factor is above 4.6, indicating unconditional stability of the amplifier. In Fig. 9(d), the relationship between output power and input power illustrates the circuit's capability to handle up to 40 dBm.

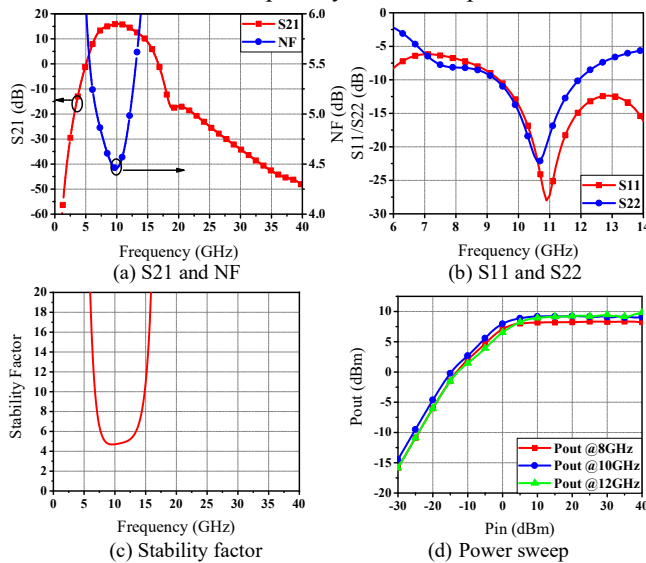


Figure 9. Simulation results of the filtering-limiter LNA.

Table I summarizes the simulated performance of the proposed filtering-limiter LNA and compares it with existing limiter LNAs. Compared to GaAs-based limiters [2-4], the IL of this design is weaker, primarily due to the inclusion of a filtering network, which deteriorates IL performance. However, compared to GaAs-based filtering-limiter [5], this design exhibits a slight IL advantage. Although the CMOS-based circuit proposed in this paper shows lower performance in terms of gain and NF compared to GaAs technology, it offers comparable power handling capability, significantly lower power consumption, and a smaller chip area. In addition, CMOS technology also provide higher integration, low cost,

offering significant advantages for realizing fully integrated RF front-end systems compared to compound semiconductor technology.

TABLE I
THE COMPARISON OF LIMITER-LNAs

Ref.	[2]	[3]	[4]	[5]	This work
Tech.	0.1μm GaAs	0.15μm GaAs	0.15μm GaAs	GaAs	180 nm CMOS
Freq (GHz)	28-38/30-38	30-36	30-38	35	8-12
Limiter IL (dB)	0.3/0.5 [^]	0.45	0.6 [^]	1.67 [#]	1.5 [#]
Gain (dB)	21/18	18.5	17	\	16
NF (dB)	2.3/2.5	2.5	2.6	\	4.5
Power Capacity (dBm)	33/37	39	38	40	40
P _{DC} (mW)	112/100	72	76	\	24
Area (mm ²)	3.38	2.1	3	0.99	0.55 [*]

[^] Estimated values from papers. [#] At the center frequency. ^{*} Core area.

IV. CONCLUSION

This paper introduces an X-band filtering-limiter LNA designed using 180 nm CMOS technology. The filtering-limiter section achieves a power handling capacity of 40 dBm. The LNA section utilizes CS and cascode structures, incorporating techniques such as shunt-series transformer feedback and inductor added in the cascode stage to enhance LNA performance. Ultimately, the filtering-limiter LNA has high power capacity, small area, and low power consumption.

ACKNOWLEDGMENT

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