

A High-Gain Low-Power Low-Noise CMOS Transconductance Amplifier

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Abstract—To achieve high gain, low power consumption and low noise, An operational transconductance amplifier(OTA) connecting folded-cascode stage and class-AB stage with translinear loops is presented in this paper. Using 180nm CMOS library in terms of the parameters, the introduced OTA exhibits a transconductance gain of 112dB, the gain bandwidth of 4.9MHz, and the input referred noise of $5.1\mu V_{rms}$ in the 1-100Hz range. The entire transconductance amplifier circuit consumes $28\mu W$ of power from a 1.8V supply when the bias source provides a current of $0.25\mu A$ and the input bias voltage is 900mV.

Keywords—High-Gain, Low-Power, Translinear Loop, OTA, CMOS

I. INTRODUCTION

Operational Transconductance Amplifiers (OTAs) have become an essential building block in various analog and mixed-signal integrated circuits. In recent years, researchers worldwide have been striving to improve the performance of OTA in terms of low power consumption, low noise and high gain. One of the good choices in OTA design is the utilization of new circuit topologies such as the telescope and folded-cascode amplifiers, which have shown significant improvements in gain and bandwidth [1]. Another promising approach is the subthreshold MOSFETs to achieve ultra-low-power operation [2]. Additionally, several researchers have proposed the use of body biasing techniques to improve linearity and enable amplifiers in low-power environments [3].

In this paper, a two-stage OTA consisting of a folded-cascode stage and a class-AB stage is designed using 180nm CMOS process. The proposed design achieves low power consumption, low noise and high gain under low voltage operating conditions and is suitable for various applications.

The folded-cascode amplifier in the first stage provides a high input impedance, thereby reducing the power consumption of the circuit. The second stage class-AB will improve the linearity of the amplifier, resulting in a higher gain. Using a translinear loop between two stages allows for better matching and isolation. Additionally, replacing resistors in the bias circuit and Miller compensation of output stage with MOSFETs not only eliminates thermal noise in high-temperature environments, but also reduces the layout area of the circuit, which is wonderful for integrated circuit design. Overall, this design strikes a balance between power consumption, noise and gain, making it suitable for a wide range of applications in low-power and high-gain analog and mixed-signal integrated circuits.

In the following sections, section II discusses some traditional design considerations, while section III analyzes the proposed OTA's topology and performs small-signal analysis. Section IV explains the simulation implementation of the proposed OTA and analyzes the simulation results. This paper is concluded in section V.

II. CONVENTIONAL OTA DESIGNS

A. The resistive self-biasing structure and Miller compensation structure with resistor

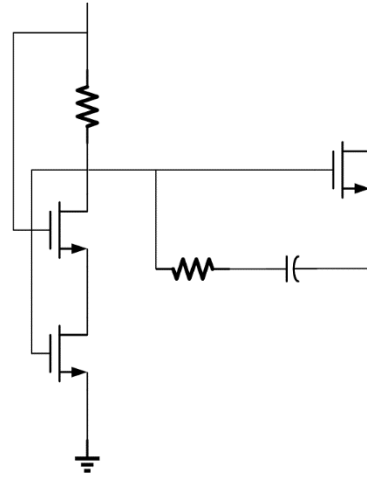


Fig.1. The traditional structure with resistor

Figure 1 shows the classic resistive self-biasing structure and resistive Miller compensation link with resistor. In low-power circuit, the quiescent current with a microampere scale will generate the voltage drop requiring a large resistance. Equations (1)~(3) are the expressions of resistive thermal noise, MOSFET thermal noise and scintillation noise. Obviously, once the resistance is determined, the resistive noise cannot be adjusted at high temperature. The thermal noise and scintillation noise of the transistor can be changed respectively by adjusting the transconductance and $W \cdot L$, the adjustment of two parameters can be achieved by changing size. At the same time, MOSFET instead of large resistance will relief the effect of resistance on the circuit.

$$(\overline{V_n^2})_R = 4kTR \quad (1)$$

$$(\overline{V_n^2})_{MOS,T} = \frac{8kT}{3g_m} \quad (2)$$

$$(\overline{V_n^2})_{MOS,F} = \frac{k}{C_{ox}WL} \cdot \frac{1}{f} \quad (3)$$

B. The Cascode Differential Pair

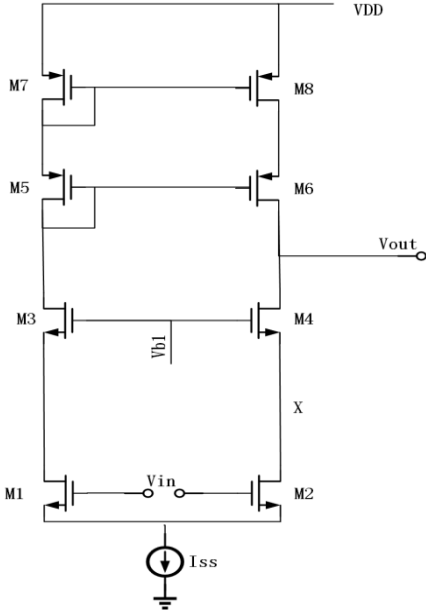


Fig.2. Cascode Differential Pair

Figure 2 shows a classic design of a sleeve-type cascode differential pair, which has a high gain and two obvious drawbacks. One weakness is the relatively small common-mode input range and output swing, which is

intuitively caused by the working range of the transistors being compressed. The output swing expression for this design is given by (4). The condition for obtaining the equation is that the common-mode input $V_{in,CM}$ is sufficiently low, the bias V_{b1} will reduce, and the bias V_{b2} is sufficiently high, which is a quite demanding synthesis condition. Another is that implementing a unity-gain buffer in the way of input-output short-circuiting is difficult, as concluded from (5), which requires transistors M_2 and M_4 to operate in saturation. The derivation of this conclusion is not elaborated here.

$$V_{OUT} = V_{DD} - (V_{OD2} + V_{OD4} + V_{ISS} + |V_{OD6}| + |V_{OD8}|) \quad (4)$$

$$\begin{cases} V_{out} \leq V_X + V_{TH2} \\ V_{out} \geq V_{b1} - V_{TH4} \end{cases} \quad (5)$$

III. THE PROPOSED OTA

A. OTA Topology

Figure 3 shows the entire circuit structure including the bias circuit. To achieve greater output swing, better linearity, and more outstanding open-loop gain, the design uses a two-stage OTA structure. The first stage is a folded-cascode structure, and the output is a class-AB stage. The two stages are bonded by a translinear loop. Because of the lower carrier mobility and higher impedance, PMOS are used in both the input pair and the tail current tubes to reduce noise.

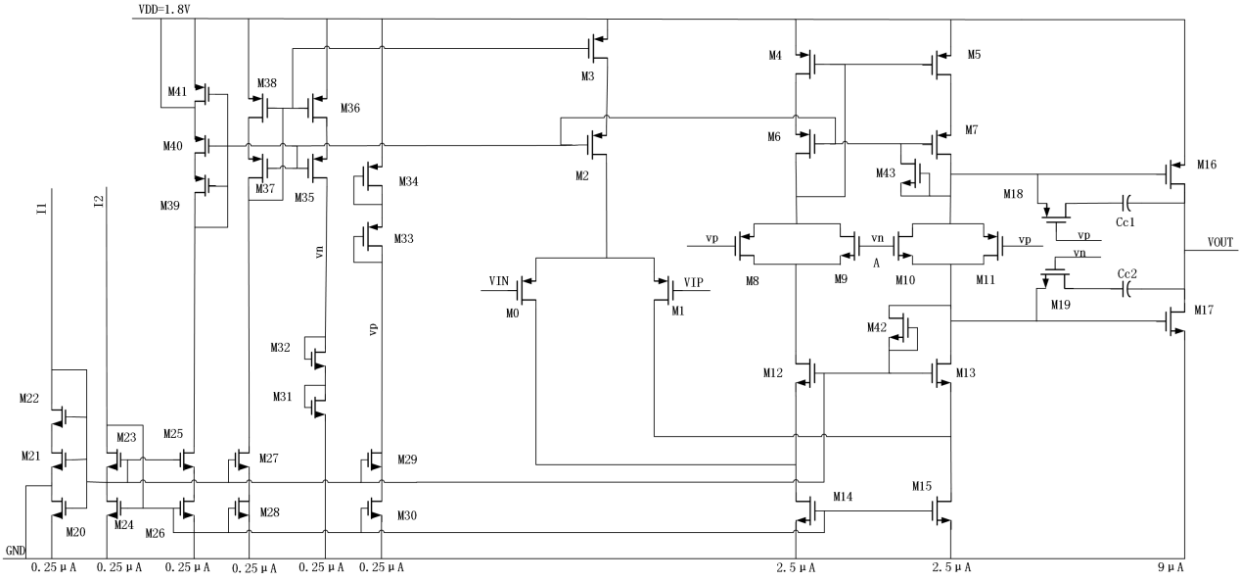


Fig.3. The Topology of The Proposed OTA

From point A's perspective, the voltage difference between it and the ground is represented by (6). Therefore, from the view of the branch of the NMOS transistor, changing the width-to-length ratio of M_{10} and M_{33} to make $V_{gs10} = V_{gs32}$ can achieve the adjustment of the gate-source voltage of M_{17} , thereby achieving the purpose of setting the bias circuit's DC operating point and reducing the current of the class-AB output stage branch, ultimately achieving low power consumption. There is a gate-source shorted clamp diode between the gate and drain of transistor M_7 and M_{13} . It is normal in a cut-off state. When the gate voltage of M_{16} drops below a certain value, transistor M_{43} turns on in the forward direction, and the limited voltage drop across it is used to clamp the gate voltage of M_{16} ,

preventing excessive current flow and high power dissipation. This approach is particularly effective in relatively high voltage operating environments, and can be deactivated under low voltage. Class-AB stage uses Miller compensation, and two MOSFET resistors are employed instead of regular resistors to reduce the input referred noise of the circuit under high temperature working conditions. In addition, the bias eliminates the structure of resistor self-biasing, which allows the lower transistor M_{21} to enter the linear region and provide channel length modulation for the upper MOSFET M_{22} , acting as a resistor. According to equation $I = P \frac{W}{L} V_{OV}^2$, adjusting L can achieve bias voltage adjustment. Moreover, at a constant current, the threshold voltage variation can dynamically balance the source

potential of M_{22} , thereby reducing the impact of body effect. Transistors M_{21} and M_{22} subject to the constraint conditions shown in (7)~(9) when operate normally.

$$V_{gs10} + V_{gs17} = V_{gs32} + V_{gs31} \quad (6)$$

$$V_{g21} = V_{g22} = V_{d22} \quad (7)$$

$$V_{ds22} \geq V_{gs22} - V_{th22} \quad (8)$$

$$V_{gs21} < V_{th21} \quad (9)$$

B. AC Small Signal Analysis

Disregarding the potential system imbalance caused by differential-to-single conversion, the first stage is treated as a fully differential circuit. The differential half-circuit equivalence principle is utilized to equate the source of the input differential pair to a differential small-signal ground, and the cascode load on the PMOS side is treated as a small-signal resistance load, resulting in the equivalence of $rib \approx g_{mp2} \cdot rop2 \cdot rop1$. The equivalent folded-cascode circuit of the first stage is shown in Figure 4, and its small-signal circuit is shown in Figure 5.

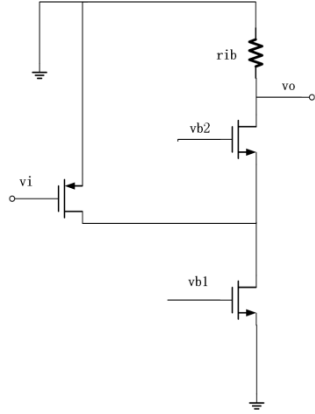


Fig.4. Equivalent folded-cascode circuit

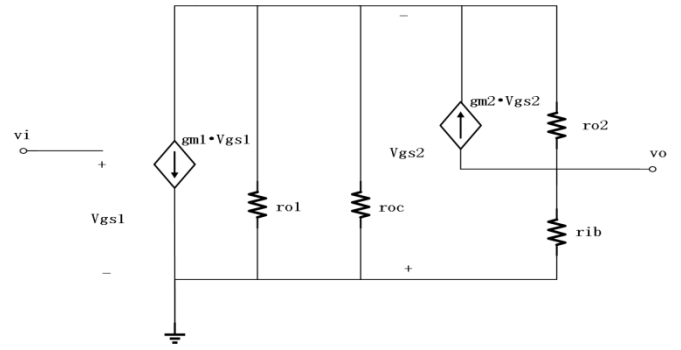


Fig.5. Small-signal circuit of the equivalent folded-cascode

To obtain the first-stage equivalent transconductance G_{m1} , the output terminal needs to be shorted to ground. Its equivalent transconductance can be expressed by (10).

$$G_{m1} = g_{m1} \quad (10)$$

To obtain the first-stage output impedance, the input needs to be grounded. Its output impedance can be expressed by (11), while (12) gives the expression for output impedance with load.

$$r_{out} \approx g_{m2} \cdot ro2(roc // ro1) \quad (11)$$

$$ro = r_{out} // rib \quad (12)$$

The gain of the first stage can be obtained by (13).

$$A_{v1} = -G_{m1} \cdot ro \quad (13)$$

By equating the folded-cascode circuit of the first stage to $G_{m1} \cdot ro$, the transconductance $G_{mab} = g_{mn} + g_{mp}$ and output impedance $roab = ron // rop$ of class-AB can be obtained. The gain of the class-AB stage can be expressed by (14). Figure 6 shows the simplified small-signal equivalent model of the entire circuit.

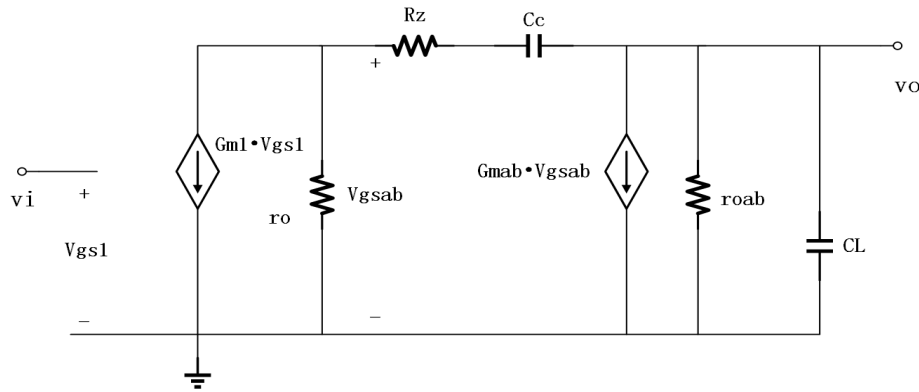


Fig.6. Simplified small-signal equivalent model

$$A_{v2} = -(g_{mn} + g_{mp})(ron // rop) \quad (14) \quad \text{expressed as below.}$$

At this point, the total open-loop gain of the circuit can be expressed by (15).

$$A_v = A_{v1} \cdot A_{v2} \quad (15)$$

According to the Miller effect, the Miller capacitor connected across the two terminals can be equivalently

$$C_i = C_C(1 + G_{mab} \cdot roab) \quad (16)$$

This capacitance is equivalent to the output of the first stage and is in parallel with the output impedance of the first stage. Due to the high-impedance node of the first stage output and the large equivalent Miller capacitance, a dominant pole is generated, which is expressed by (17).

$$p_1 = \frac{1}{[r_{o1} \cdot (1 + G_{mab} \cdot r_{oab}) C_C + R_Z \cdot C_C] \cdot 2\pi} \quad (17)$$

To simplify the model, a resistor R_Z is used to replace the diode.

The Miller capacitance is approximately C_C when equivalent to the second stage, and the output is a high-impedance node, with a subdominant pole located at the output of the second stage. With the frequency increasing, the impedance of the Miller capacitor decreases in class-AB. The Miller capacitor can be regarded as a parallel feedback that reduces the output impedance of the second stage, and the impedance reaches the minimum $\frac{1}{G_{mab}}$. The subdominant pole can be expressed by (18).

$$p_2 = \frac{G_{mab}}{(C_C + C_L) \cdot 2\pi} \quad (18)$$

For stability reasons, assuming $GBW < 0.1p_2$. That is, if the middle frequency band is wide enough and the total gain drops at 20dB/dec before GBW, then the gain bandwidth product can be expressed by (19).

$$GBW = p_1 \cdot A_v = \frac{g_{m1} \cdot r_{o1} \cdot G_{mab} \cdot r_{oab}}{[r_{o1} \cdot (1 + G_{mab} \cdot r_{oab}) C_C + R_Z \cdot C_C] \cdot 2\pi} \approx \frac{g_{m1}}{2\pi \cdot C_C} \quad (19)$$

The location of the right-half plane zero is calculated next. The output is set to zero, because what is being sought is a forward path, and the output of the first stage can be considered as a small-signal input for the zero. The right-half plane zero can be expressed by (20).

$$s = + \frac{g_{mn} + g_{mp}}{C_C} \quad (20)$$

Resistors can compensate for the right-half plane zero caused by the Miller capacitor and the second-stage transconductance. The expression for the zero with the consideration of the resistance is given by (21).

$$s = \frac{1}{C_C \left(\frac{1}{g_{mn} + g_{mp}} - R_Z \right)} \quad (21)$$

When $R_Z > \frac{1}{g_{mn} + g_{mp}}$, the zero moves to the left-half plane, which compensates for the phase. Adjusting the resistor can be considered to offset the subdominant pole and improve phase margin.

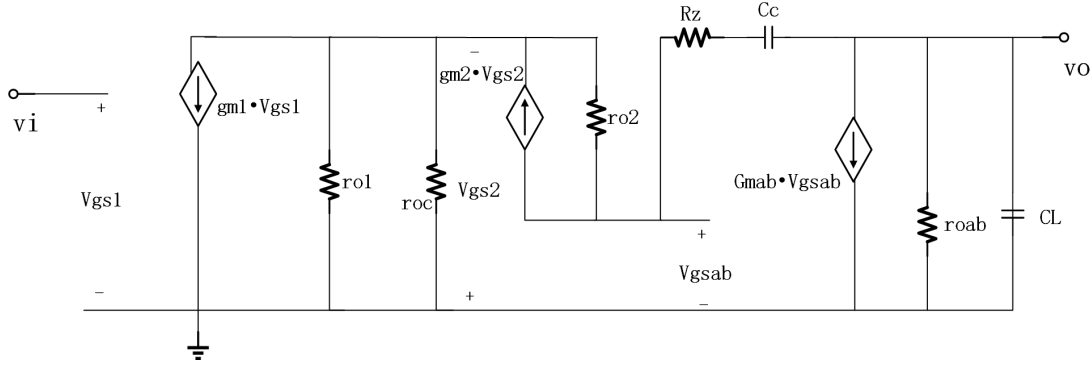


Fig.7. Equivalent small-signal model

Figure 7 shows the equivalent small-signal model of the entire circuit.

IV. SIMULATION AND ANALYSIS

The presented OTA is simulated using SMIC180nm CMOS technology parameters. When the reference current source provides 0.25μA current, the input voltage is 900mV,

and the output stage is loaded with 10pF capacitor, the whole circuit demonstrates good performance. As shown in Figure 8, the frequency response of the proposed OTA exhibits a gain of 112.6dB, a unity-gain bandwidth of 4.9MHz, and a phase margin of 65.7deg. The circuit is biased using a 1.8V voltage supply and has a power consumption of only 28μW.

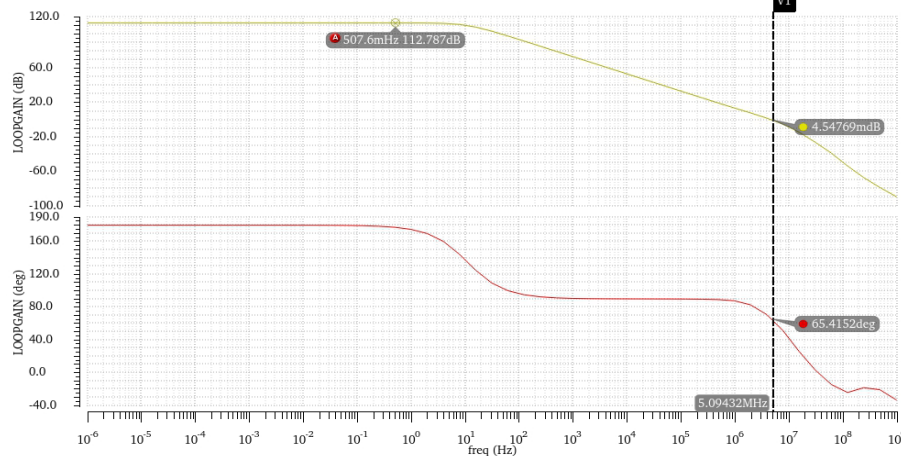


Fig.8. Frequency response

In addition, Figure 9 shows the input-noise-power spectral density of the OTA, with the input-referred noise of $5.1\mu V_{rms}$ in range of 1-100Hz. Figure 10 demonstrates a common-mode rejection ratio of 121dB. As shown in Figure 11, Monte Carlo simulations are performed considering

different process and extreme temperature conditions (-40°C and 125°C). The results show that the minimum loop gain is still as high as 98dB. The Monte Carlo simulation results are presented in Figure 12, where the offset voltage is $-102.8\mu\text{V} \pm 3\text{mV}$.

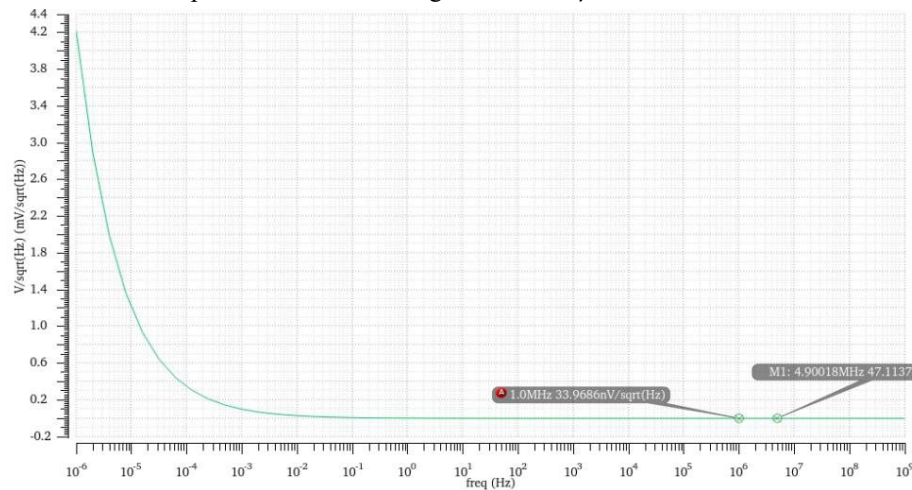


Fig.9. Power spectrum of the Input referred noise

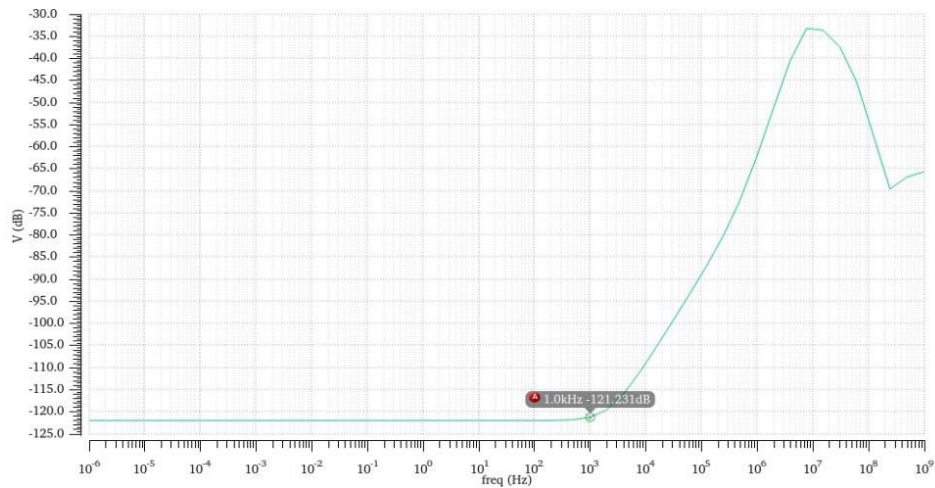


Fig.10. Simulated PSRR

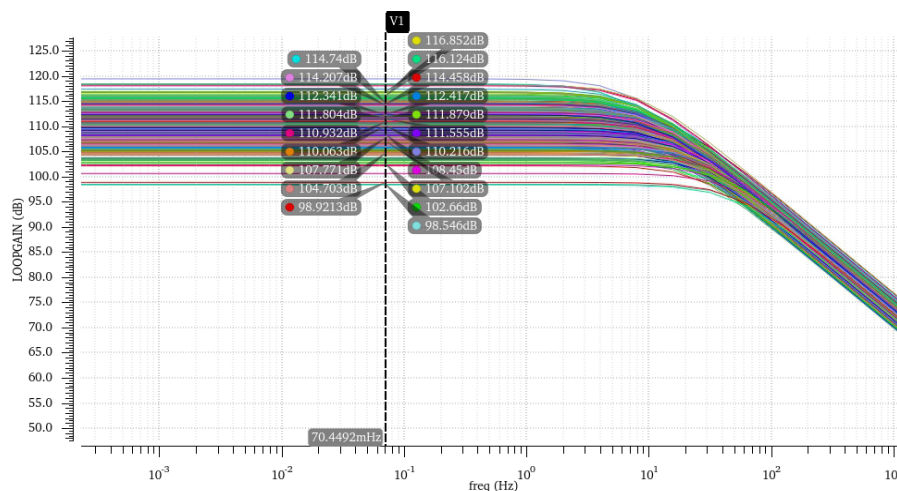


Fig.11. Frequency response in Monte Carlo simulations

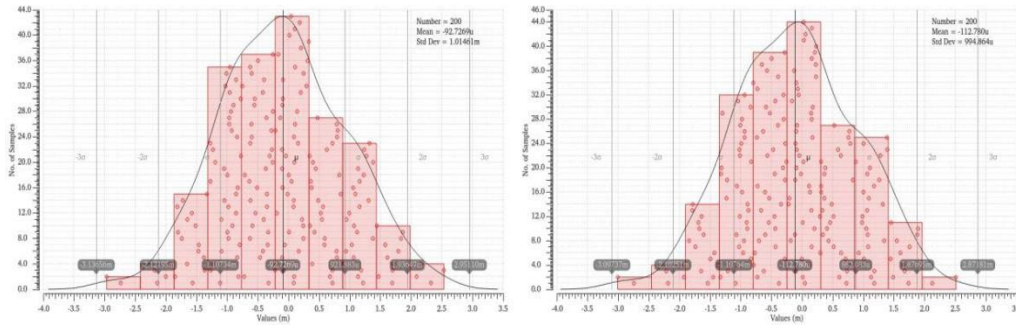


Fig.12. Offset voltage (-40°C on left, 125°C on right)

Table I shows detailed simulation results and performance parameters.

TABLE I DETAILED SIMULATED PERFORMANCE

Settling time	Slew rate	PSRR	CMRR	CMR
1.75 μ s	1.35V/ μ s	119.1dB	121.2dB	0-1.5V
Supply voltage range	Maximum load capacity	Input referred noise	Power dissipation	Quiescent current
1.38-2.41V	39.5pF	5.1 μ V _{rms} (1-100Hz)	28 μ W	15.5 μ A
GBW	Gain	Offset voltage	Phase margin	Supply voltage
4.9MHz	112.6dB	-102.8 μ V $\pm$ 3mV	65.7°	1.8V
Gain margin				
26.6dB				

Table II compares the performance parameters of the presented OTA with those of other previous transconductance amplifier designs. It can be clearly seen in

Table II that the proposed OTA has high gain, low power consumption and low noise, and obviously has better comprehensive performance.

TABLE II PARAMETER COMPARISON

Parameter	[4]	[5]	[6]	[7]	[8]	This work
Technology(μ m-CMOS)	0.13	0.18	0.35	0.18	0.18	0.18
Supply voltage(V)	1.8	$\pm$ 0.75	3.3	1.2	1.2	1.8
Gain(dB)	69.73	106.75	>80	40	-	112.6
Power dissipation(μ W)	389	397.5	<7000	24.8	27.8	28
Input referred noise	-	384nV/ $\sqrt{\text{Hz}}$ (at 1MHz)	-	1.67 μ V _{rms} (1-100Hz)	5.05 μ V _{rms} (1-100Hz)	5.1 μ V _{rms} (1-100Hz), 33.9nV/ $\sqrt{\text{Hz}}$ (at 1MHz)
CMRR(dB)	62.9	259	-	66	68	121.2
GBW(MHz)	28.4	3.72	300	-	-	4.9

Finally, the layout designed by OTA is illustrated in Figure 13.

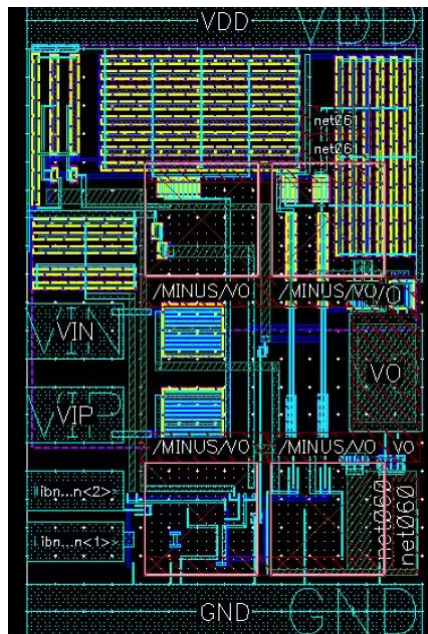


Fig.13. Layout

V. CONCLUSION

A two-stage operational transconductance amplifier with folded-cascode input stage and class-AB output stage with Miller compensation have been presented. The OTA uses a translinear loop to set the DC point of the output pair. Under the premise of fully considering power-GBW tradeoff, the circuit consumes only 28 μ W of power and GBW reaches 4.9MHz when the power voltage is 1.8V. Meanwhile, the loop gain reaches 112dB and the input noise is only 5.1 μ V_{rms} in the frequency range 1-100Hz. The simulation of the presented design is realized by SMIC180nm CMOS technology in Cadence.

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