



Ultra-wideband Low Noise Amplifier with Approach of High Linearity Using Power Derivative Technique

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Abstract

Low-noise amplifier (LNA) is a notable element in RF radio receivers to enhance the desired signal and improve the performance of the receiver. Linear property of LNA must be focused due to the existence of different noisy signals and interferers. In addition, extended linearity range leads to less harmonics generation. In this paper, 180-nm technology is used to design an efficient LNA in ultra wide-band (UWB) frequencies with high linearity and low-noise properties. The design is based on using power derivative technique which improves the linearity property and achieves lower noise figure. The simulation results show the gain of 11.125 dB with consumed power of 25.5 mW where the supply voltage is 1.5 V. Noise figure is achieved as 2.6 dB while the reflection (S_{11}) is less than -13.35 dB. IIP3 which shows the linearity characteristic is obtained as 18.599 dBm at the frequency range of UWB (3.1–10.6 GHz) which is desirable.

Keywords Low noise amplifier · Linearity · UWB · Gain · Power derivative technique

1 Introduction

In the wireless communications, the efficient receiver can be achieved considering many interferers and noise in the wireless circumstance. Low noise amplifier (LNA) is a precious element in these receivers to enhance the desired signal from the received polluted signal. In addition, the linearity range of LNA must be highly considered due to the signal delivery from LNA to the mixer in the receiver structure (Razavi and RF 2011; Daryabari et al. 2019a, 2019b).

The noise reduction is a main factor in design of an efficient LNA. Different impedance matching methods, using low-noise components and choosing low-noise circuit bias conditions are several main efforts to obtain the low-noise structure. Another main challenge of LNA design is the linearity range where many papers are focused on suggesting the solutions for this challenge. In (Im and Lee 2013), the desired LNA is proposed with the forward body bias technique to achieve the high gain and low

power consumption. By using a simultaneous source, input matching in a wide bandwidth and low noise figure (NF) has been achieved in the first stage. In the second stage, the gain enhancement in high frequencies is obtained. In (Shim and Yang 2013), an LNA in 180-nm technology is presented. The harmonic rejection method is applied by using RC feedback in the gain stage, which increases the linearity. This type of feedback is used to minimize the number of capacitors and resistors. In (Nguyen et al. 2004; Ganesan and May 2006), a differential low-noise amplifier with high linearity in 90-nm technology is presented using the derivative superposition (DS) technique. In (Mecwan et al. 2016; Zhang et al. 2009), a low noise amplifier is proposed using the double feedback technique to increase the gain. This circuit is a combination of common-gate and common-source stages. By placing an active load instead of the resistance as the local feedback, the gain enhancement and noise reduction are achieved. In (Seiedhosseinzadeh and Nabavi 2012; Hsieh et al. 2008; Moezzi and Sharif Bakhtiar 2012), a linear low noise amplifier has been designed and simulated using 180-nm technology at the frequency range of 5 GHz. In this paper, infrared matching (IM) is used at the desired frequency where IIP3 is improved compared to the conventional LNA. In (Pandey and Singh 2015; Yoon and Park 2014; Parvizi et al. 2014),

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the design of ultra wide-band (UWB) low noise amplifier in 180-nm technology using post distortion linearization technique is suggested. Common-gate structure is employed where using an auxiliary PMOS leads to the cancellation of the second and third harmonics of nonlinear currents. The gain and noise figure are slightly improved while a three-dimensional passband Chebyshev filter is presented for input matching. In (Gao et al. 2015; Bastos et al. 2016), the linearity of the low-noise amplifier is improved by using the feedback method at the frequency of 5.8 GHz. The feedback technique is applied by using a transistor to increase the linearization of the circuit, where the gate voltage is controlled by the bias circuit. In (Li et al. 2014a; Ehsan Kargaran¹, Mohsen Jamshidi², Abbas Z. Kouzani³, and Khalil Mafinezhad, A xxxx; Benqing Guo and Xiaoleili 2013), a low noise amplifier with linearity and proper input matching at the frequency of 2.4 GHz with 130-nm technology is designed based on the input matching circuit and the basic structure of common-gate. In (Khaleel and Abbas 2017; Kim et al. 2010; Aditi 2010), an ultra wide-band low noise amplifier is simulated using two improved complementary derivative superposition techniques and forward body bias technique. Taken high linearity technique for ultra-wideband low noise amplifier in 180-nm CMOS technology is proposed in Andrew et al. xxxx; Siamak.v., mostafa.Y. xxxx; Galal et al. xxxx) where design and analysis of 28 GHz CMOS low-power LNA with 6.4 dB gain variability for 5G applications is presented. Post distortion star feedback method is employed to achieve the highly linear LNA in these papers.

In this paper, power derivative and derivative superposition are proposed to present an efficient LNA. In this scheme, common-gate is used and by combining these strategies, the linearity is notably improved. The main contributions of the paper can be summarized as follows:

- Applying power derivative method to suppress the third harmonic signal
- Applying derivative superposition in the proposed structure to extend the linearity range
- Using common-gate and Cascode structure to achieve high gain and low noise amplifier
- Implementing an efficient matching circuit in input stage for supporting of wide range of UWB

The rest of the paper is as follow. In Sect. 2, the proposed structure is completely described in details. In Sect. 3, the complete analysis of the proposed LNA in terms of gain, noise, matching and IIP3 is presented. Simulation and layout results are discussed in Sect. 4 where some conclusions are provided in Sect. 5.

2 Proposed Structure

In this section, the designed LNA based on linearity range extension and desirable gain is proposed in Fig. 1. The proposed circuit is designed in 180-nm technology where matching circuits are used both in input and output parts. The value of elements is described in Table 1.

The use of common-source (CS) architecture in the first stage and employing the inductor L_3 in the source result in the input matching where the noise figure is reduced. Figure 2 shows the cascode structure used in the proposed design. The capacitive property of the input impedance of this part is low due to the low value of the C_{gs} of M_1 and thus, the matching resonance frequency will occur at the frequencies higher than our desired bandwidth. By adding the inductor L_2 (as shown in Fig. 3) and reducing the resonance frequency, it can be seen that the matching is obtained in the desired UWB frequencies while the gain loss is compensated in this part.

The next step of the design is focused on the lower bandwidth region. For matching at low frequencies, another resonance is required, which can be achieved by adding capacitor C_2 in the first stage between gate and drain of M_1 (see Fig. 1). The effect of adding C_2 on the noise figure of the structure is presented in Fig. 4. Moreover, the inductor L_4 in M_2 can be applied to resonate with L_5 and the parasitic capacitor, C_{gd} of M_2 which leads to the compensation of gain reduction in the high frequencies and achievement of the desired bandwidth. In the second stage, power derivative (PD) method is used as the main novelty of the proposed structure. In this technique, increasing v_{gs} leads to the change of the third-order distortion component (gm_3) from positive value to the negative one. Therefore, using the fact of the similarity of both bias circuits and currents, the third harmonic component is reduced and thus, the linearity range of the proposed structure is notably extended. Thus, high linearity is provided and IIP3 parameter is improved. Without using this method in the second stage, IIP3 is low while applying PD strategy causes improving the linearity property and achieving higher IIP3 as discussed in the next sections. L_6 and C_4 are also employed in the output of the second stage for obtaining flatter gain which is shown in Fig. 5. Globally stating, using the proposed structure causes higher linearity range and smoother gain which are desirable goals of this paper.

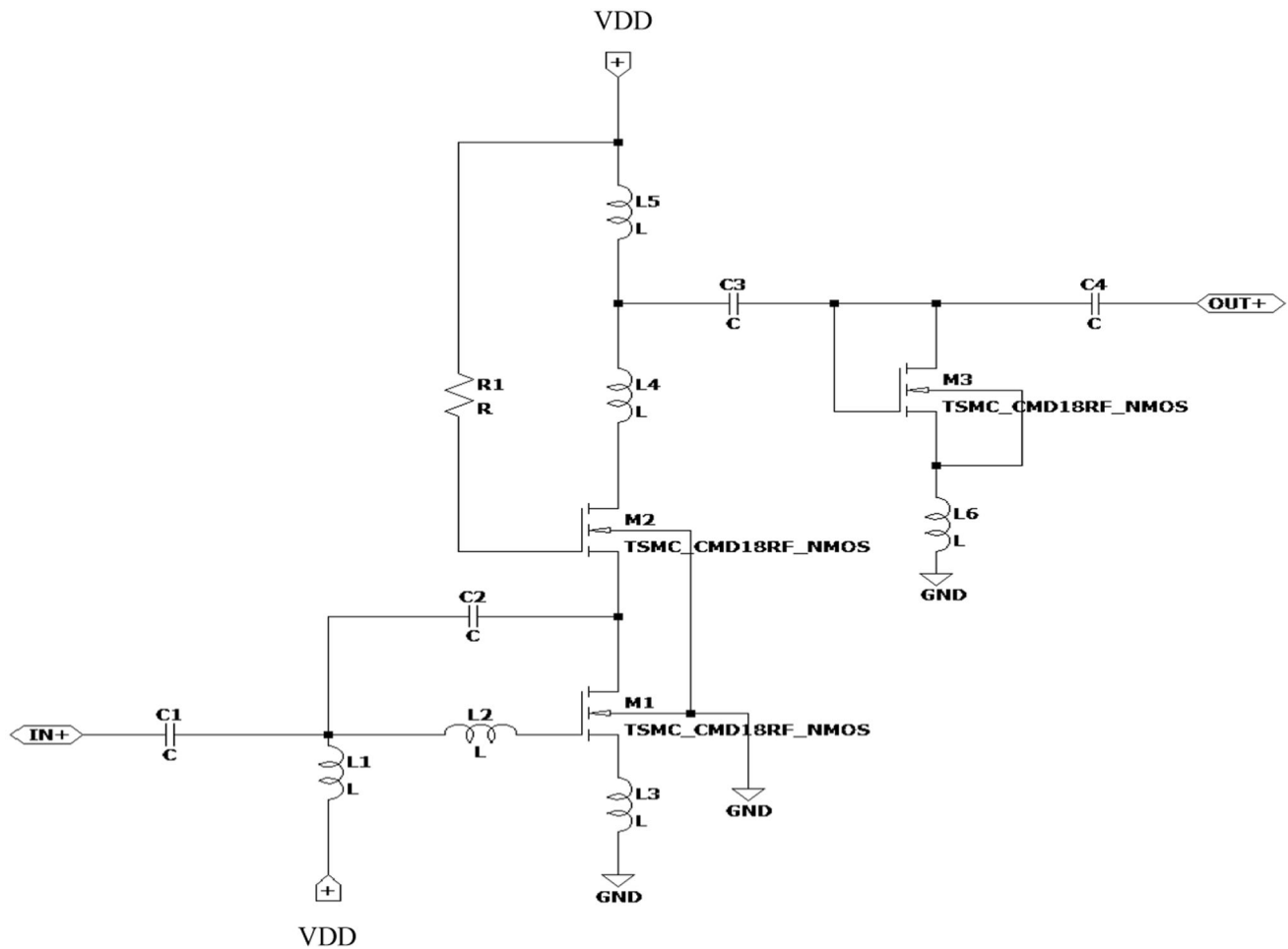


Fig. 1 Schematic of the proposed LNA

Table 1 Value of elements of the proposed LNA

Value	Element	Value	Element
500 Pf	C1	2.23 nH	L1
375 Ff	C2	1.2 nH	L2
440 fF	C3	482 pH	L3
606 pF	C4	3.18 nH	L4
W = 100 u	M1	4.7 nH	L5
W = 100 u	M2	61.3 nH	L6
W = 250 u	M3	5 Ω	R

3 Analysis of the Proposed LNA

3.1 Gain Analysis

The gain analysis of the proposed LNA is discussed as follow. The small-signal model of the proposed structure is shown in Fig. 6 where by writing KCL in the source of M_1 , we have:

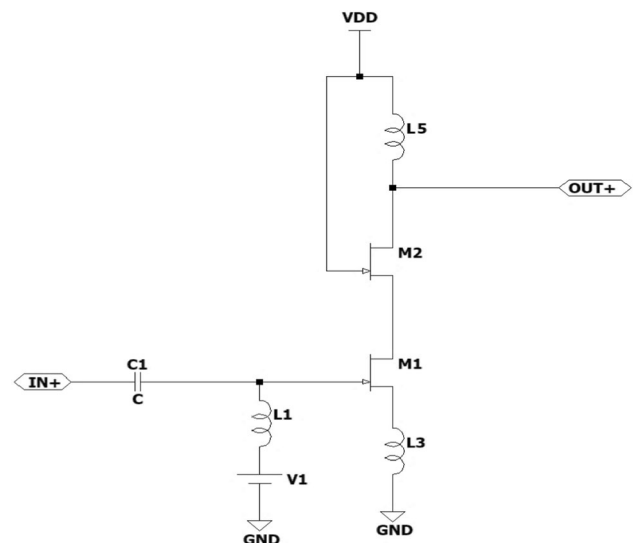


Fig. 2 Schematic of cascode structure

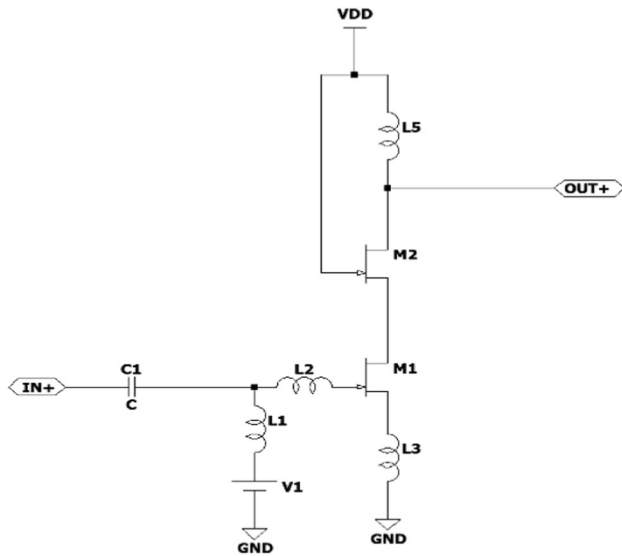


Fig. 3 Schematic of the cascode structure adding L_2

$$\frac{v_{s1}}{sL_3} + \frac{v_{s1} - v_{g1}}{\frac{1}{sC_{gs}}} = g_{m1}v_{g1} - g_{m1}v_{s1} \quad (1)$$

$$v_{s1} \left(\frac{1}{sL_3} + sC_{gs1} + g_{m1} \right) = v_{g1} (sC_{gs1} + g_{m1}) \quad (2)$$

$$v_{s1} = \frac{(sC_{gs1} + g_{m1})}{\left(\frac{1}{sL_3} + sC_{gs1} + g_{m1} \right)} v_{g1} \quad (3)$$

$$\text{Assuming } A = \frac{(sC_{gs1} + g_{m1})}{\left(\frac{1}{sL_3} + sC_{gs1} + g_{m1} \right)}, \text{ we have:} \quad (4)$$

$$v_{s1} = A \bullet v_{g1}$$

Next, by writing KVL in M_1 , we have:

$$\frac{v_{in}^\circ - v_{g1}}{sL_2} = \frac{v_{g1} - A \bullet v_{g1}}{\frac{1}{C_{gs1}}} \quad (5)$$

$$\frac{v_{in}^\circ}{sL_2} = \left(sC_{gs} - A \bullet sC_{gs} + \frac{1}{sL_2} \right) v_{g1} \quad (6)$$

Assuming $B = \frac{1}{(s^2 C_{gs2} L_2 (1-A) + 1)}$, then we have:

$$v_{g1} = B \bullet v_{in}^\circ \quad (7)$$

By writing KCL in the source of M_1 , we have:

$$\frac{v_o^\circ}{\frac{1}{sC_{gs}} + sL_4} = (v_o^\circ - v_{in}^\circ) C_2 s + g_{m1} v_{gs1} \quad (8)$$

By replacing (4) and (7) in (8), we have:

$$\left[\frac{sC_{gs2}}{s^2 C_{gs2} L_4 + 1} - sC_2 \right] v_o^\circ = B \bullet (1 - A) g_{m1} v_{in}^\circ \quad (9)$$

Since, M_3 is designed as a current source circuit, it will act as a resistance in the small-signal mode. Thus, due to

(9), assuming $C = \frac{B \bullet (1-A) g_m}{\left(\frac{sC_{gs2}}{s^2 C_{gs2} L_4 + 1} - sC_2 \right)}$ and some simplifications,

we finally have the gain as:

$$v_o^\circ = C \bullet \frac{-g_m R L_6 S}{L_6 S + \frac{1}{C_s} + R} \bullet \frac{1}{L_4 C_{gs} s^2 + 1} \bullet \frac{v_{in}^\circ}{\left(R_s + \frac{1}{sC_1} \right) [sC_2 + B \bullet sC_{gs1} (1 - A) - C]} \quad (10)$$

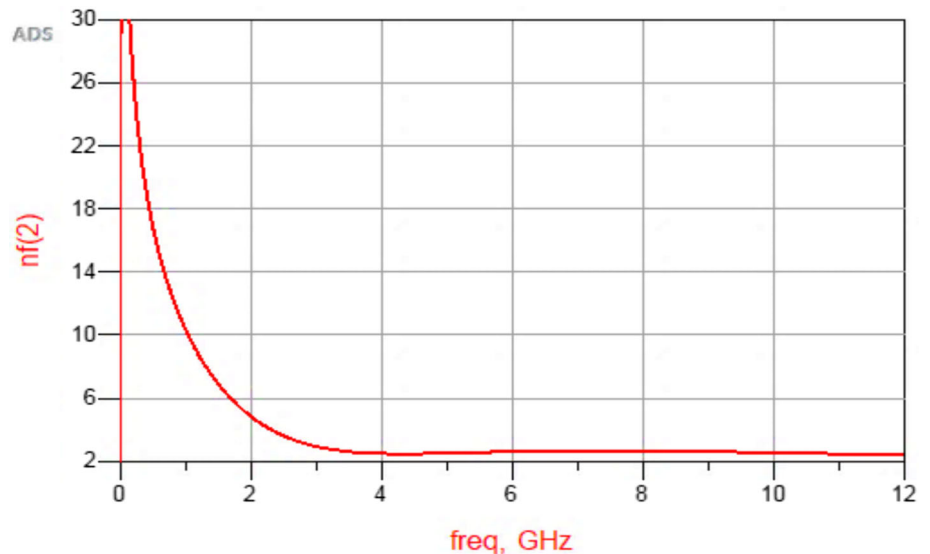
3.2 Input Matching

Matching circuit is needed to obtain the input reflection, S_{11} lower than -10 dB, which is desirable (Li et al. 2014b).

The analysis of input matching can be described as below.

To calculate the input impedance, we have:

Fig. 4 Noise figure after adding capacitor C_2 in the first stage of the proposed LNA



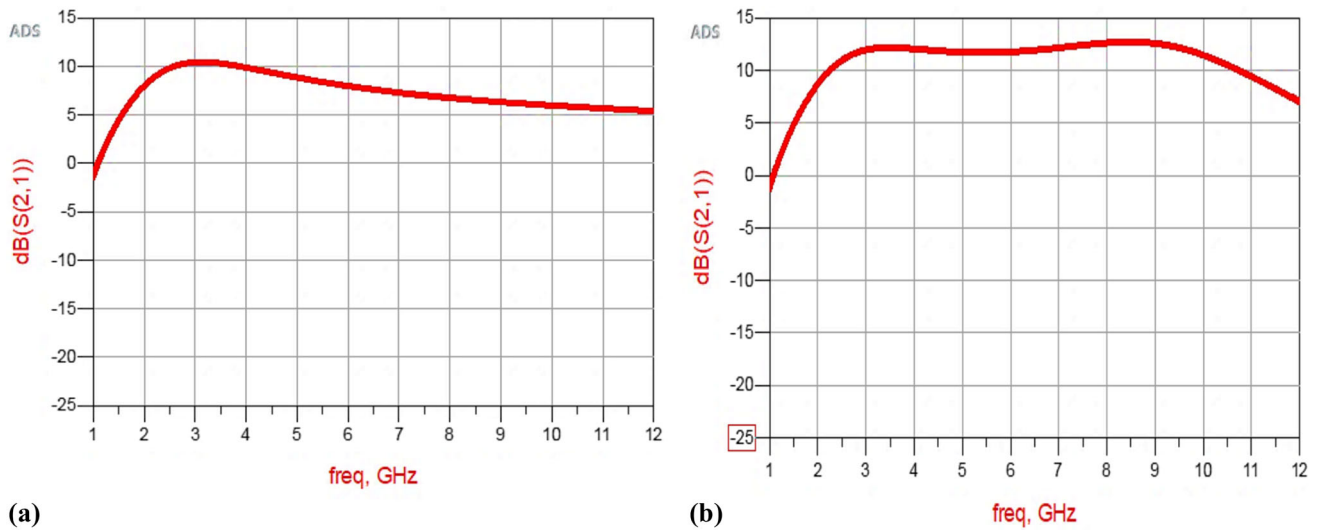


Fig. 5 a The effect of applying L_6 and C_4 on the gain (before applying). b The effect of applying L_6 and C_4 on the gain (after applying)

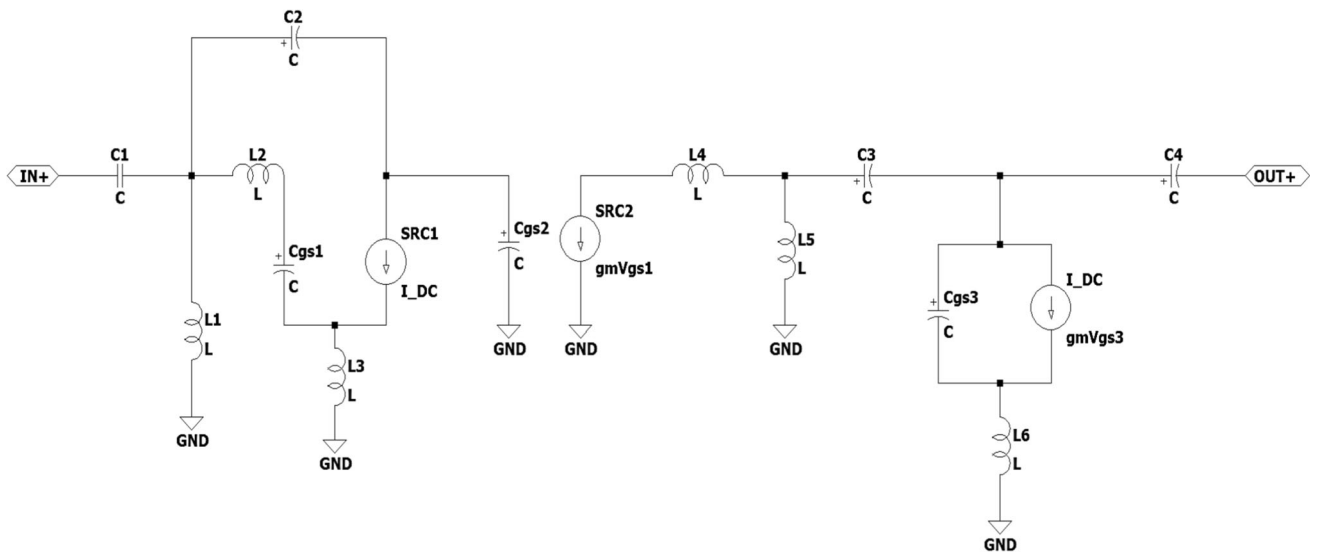


Fig. 6 Small-signal model of the proposed LNA

$$V_T = A \bullet v_{gs1} \quad (11)$$

$$A = (L_1 C_{gs1} s^2 + 1 + L_2 s (g_{m1} + C_{gs1} s)) \quad (12)$$

$$V_T = \left(Z_X + \frac{1}{C_4} \right) I_T + \frac{B}{A} V_T \quad (13)$$

$$B = \frac{C_{gs1}}{C_4} + (g_{m1} + C_{gs1} s) Z_X \quad (14)$$

$$Z_T = \frac{V_T}{I_T} = \frac{Z_X + \frac{1}{C_4}}{1 - \frac{B}{A}} \quad (15)$$

where Z_X is the impedance viewed from the output which is parallel to C_4 .

3.3 Noise Analysis

The small-signal model for noise analysis is depicted in Fig. 7. The noise analysis is done in three parts where the model of the first part is depicted in Fig. 8. In this model, the input voltages (v_g^2, v_s^2) are transferred to the output with the gain G_m^2 . The noise of i_d^2 must be applied where the activation of g_m causes parallel noise with i_d^2 . The current noise calculation in the source is given as below (Wang et al. 2016):

$$v_\pi = -(g_m v_\pi + i_d) \times \frac{j\omega L_s}{j\omega L_s + \frac{1}{j\omega C_{gs}} + j\omega L_g + R_s} \times \frac{1}{j\omega C_{gs}} \quad (16)$$

Fig. 7 Noise equivalent circuit of the proposed structure

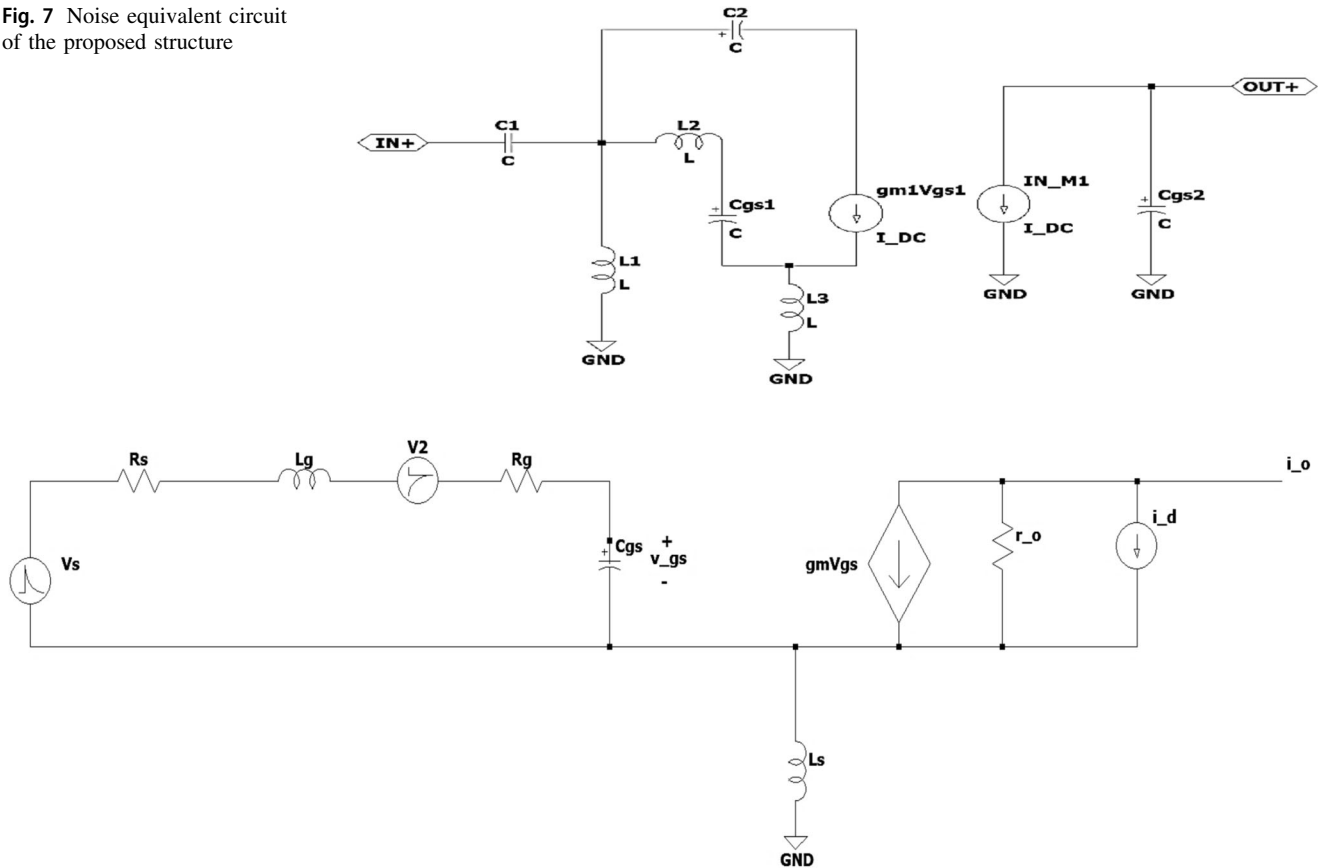


Fig. 8 Noise equivalent model of the first stage (CS part) of the proposed LNA

At the resonance frequency, the denominator is simplified to R_s and we have:

$$v_\pi = -(g_m v_\pi + i_d) \frac{j\omega L_s}{R_s j\omega C_{gs}} = -(g_m v_\pi + i_d) \frac{L_s}{R_s C_{gs}} \quad (17)$$

$$v_\pi \left(1 + \frac{L_s g_m}{R_s C_{gs}}\right) = -(i_d) \frac{L_s}{R_s C_{gs}} \quad (18)$$

According to $\omega_T L_s = R_s$, we have:

$$2v_\pi = -(i_d) \frac{L_s}{R_s C_{gs}} \quad (19)$$

$$g_m v_\pi = \frac{-i_d}{2} \frac{g_m L_s}{C_{gs} R_s} = \frac{-i_d}{2} \quad (20)$$

$$\overline{i_{o,T}^2} = G_m^2 \left(\overline{v_s^2} + \overline{v_g^2} \right) + \frac{1}{4} \overline{i_d^2} \quad (21)$$

It is observed that only 25% of the internal noise is transferred to the output. Thus, the total output noise is expressed as below:

$$F = 1 + \frac{\overline{V_g^2}}{v_s^2} + \frac{\overline{i_d^2}}{4v_s^2 G_m^2} \quad (22)$$

where finally, we have:

$$F = 1 + \frac{R_g}{R_s} + \frac{\left(\frac{\gamma}{2}\right) g_m (2R_s)^2}{4R_s} \left(\frac{\omega}{\omega_T}\right)^2 \quad (23)$$

In consequence, the noise of cascode structure is assessed where the equivalent circuit is shown in Fig. 9. From this figure, we have:

$$v_\pi = (g_m v_\pi + i_d) \frac{1}{j\omega C_{gs}} \quad (24)$$

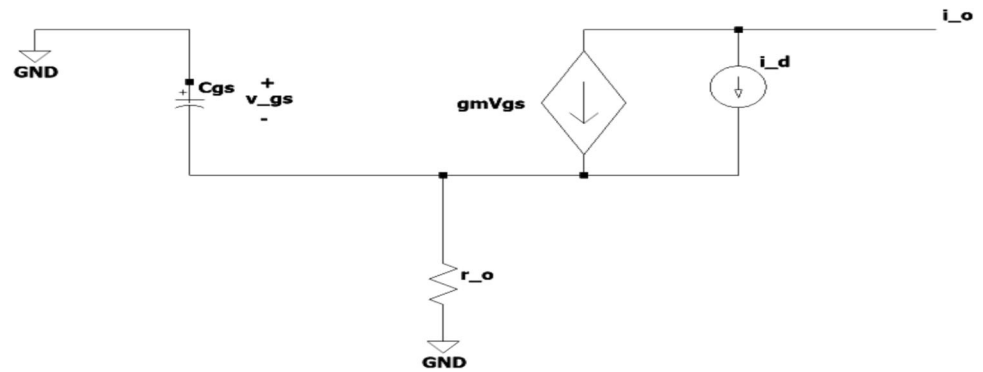
$$(v_\pi (j\omega C_{gs} - g_m v_\pi) = i_d) \quad (25)$$

$$g_m v_\pi = \frac{-g_m}{g_m - j\omega C_{gs}} i_d = \frac{-i_d}{1 - j\frac{\omega}{\omega_T}} \approx -i_d \quad (26)$$

Since the gain of the cascode structure is high, the noise of M_3 can be ignored. Therefore, only the noise of M_1 is calculated. Thus, we have:

$$v_\pi (j\omega C_{gs} - g_m v_\pi) = -v_\pi \quad (27)$$

Fig. 9 Noise equivalent circuit of cascode structure



$$i_d r_o = -v_\pi - g_m r_o v_\pi = -(1 + g_m r_o) v_\pi \quad (28)$$

$$v_\pi = \frac{-r_o}{1 + g_m r_o} i_d \quad (29)$$

$$g_m v_\pi = \frac{-g_m r_o}{1 + g_m r_o} i_d \approx -i_d \quad (30)$$

Finally, the output noise of the cascode part can be resulted as:

$$\left(1 - \frac{-g_m r_o}{1 + g_m r_o}\right) i_d = \left(1 - \frac{1}{1 + g_m r_o}\right) i_d \approx 0 \quad (31)$$

In the above analysis, the noise power of the cascode structure can be neglected the same as the noise power of M_3 . The noise of M_1 can be presented as:

$$I_O = \frac{v_o^\circ - v_{in}^\circ}{\frac{1}{sC_2}} + g_{m1} v_{gs} + I_{n,M1} \quad (32)$$

I_o shows the current due to the trans-conductance of the circuit and we have:

$$I_O = \frac{v_o^\circ}{\frac{1}{sC_{gs}}} \quad (33)$$

Assuming $D = \frac{1}{sC_{gs}}$:

$$v_o^\circ = D \cdot I_O \quad (34)$$

Considering

$$E = \left(R_s + \frac{1}{sC_1}\right) [sC_2 + B \cdot sC_{gs1}(1 - A) - C] \text{ and } I_O = \frac{v_o^\circ}{\frac{1}{sC_{gs}}}, \text{ we have:}$$

$$I_O = \frac{D \cdot I_O - E \cdot v_{in}}{\frac{1}{sC_2}} + BE(1 - A) \cdot g_{m1} v_{in} + I_{n,M1} \quad (35)$$

$$v_{in}(sC_2 \cdot E + BE(1 - A) \cdot g_m) = I_O(1 - D \cdot sC_2) - I_{n,M1} \quad (36)$$

$$\rightarrow v_{in} = \frac{(1 - D \cdot sC_2)}{(sC_2 \cdot E + BE(1 - A) \cdot g_m)} I_O - \frac{1}{(sC_2 \cdot E + BE(1 - A) \cdot g_m)} I_{n,M1} \quad (37)$$

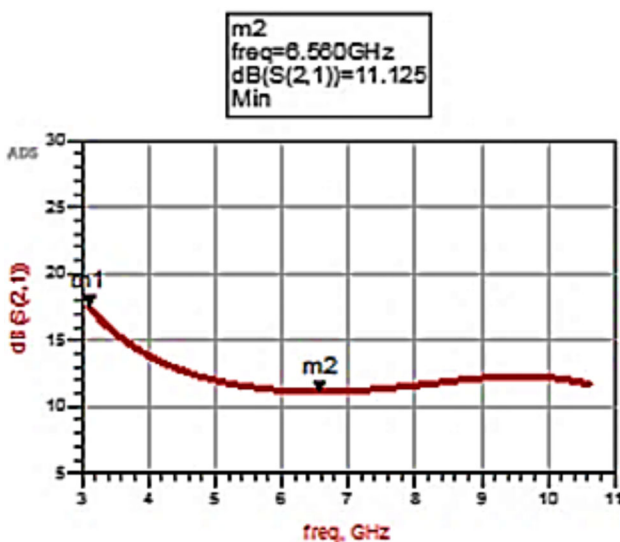


Fig. 10 Gain simulation of the proposed structure

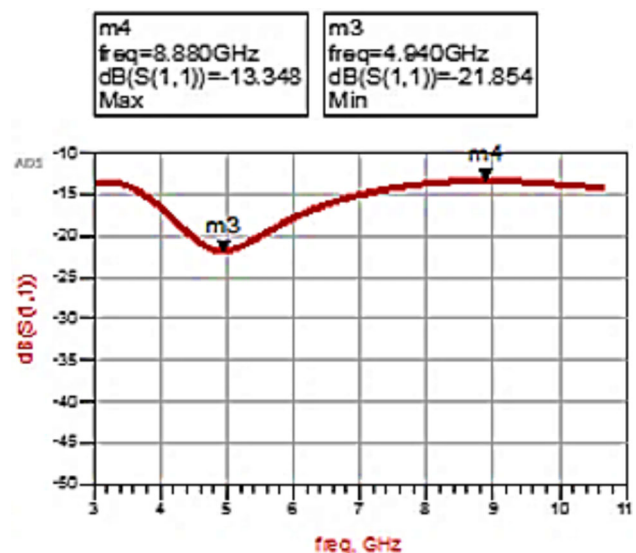


Fig. 11 Input matching property of the proposed LNA

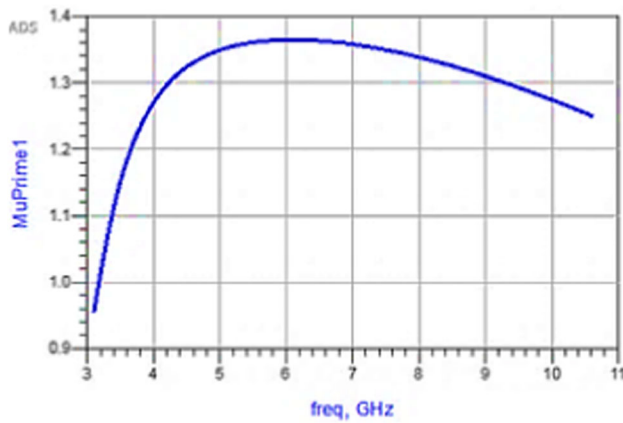


Fig. 12 Stability parameter of the proposed LNA

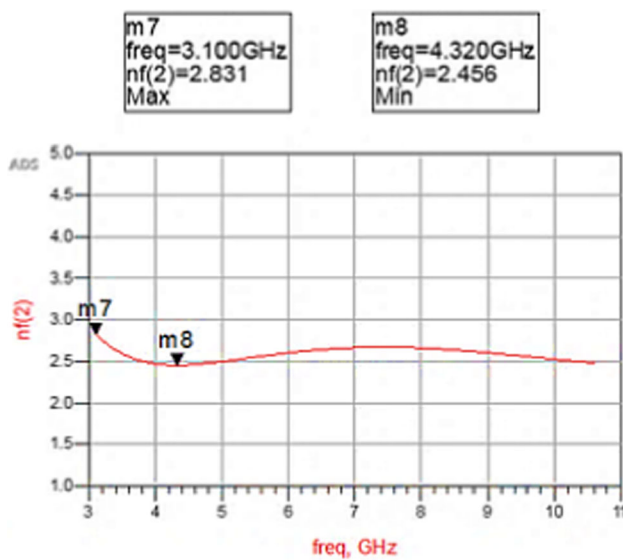


Fig. 13 NF of the proposed LNA

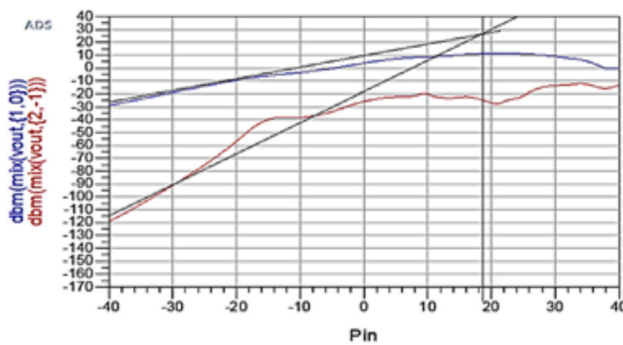


Fig. 14 IIP3 parameter of the proposed LNA

$$\left| \frac{I_O}{v_{in}} \right| = \frac{(sC_2 \bullet E + BE(1 - A) \bullet g_m)}{(1 - D \bullet sC_2)} \quad (38)$$

Thus, the output noise of M_1 can be described as:

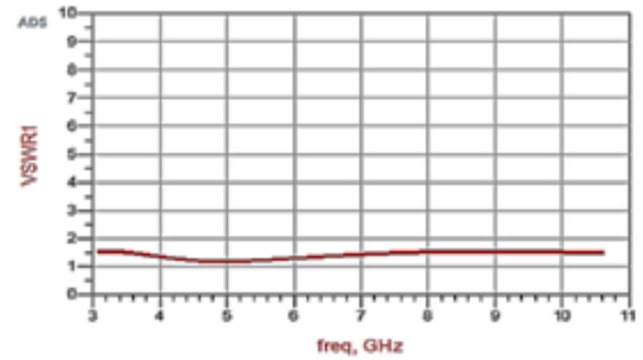


Fig. 15 VSWR parameter of the proposed LNA

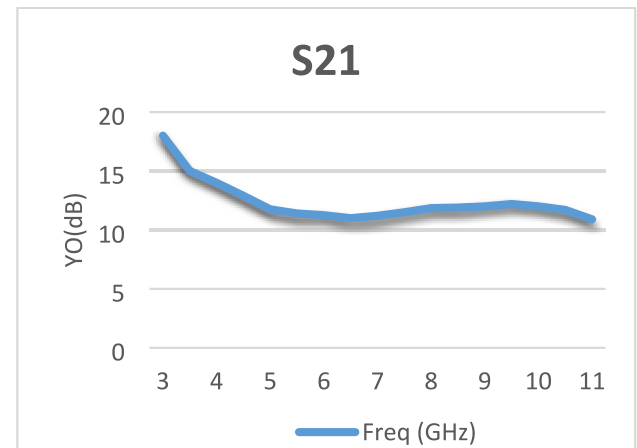


Fig. 16 Gain result of the post-layout of the proposed LNA

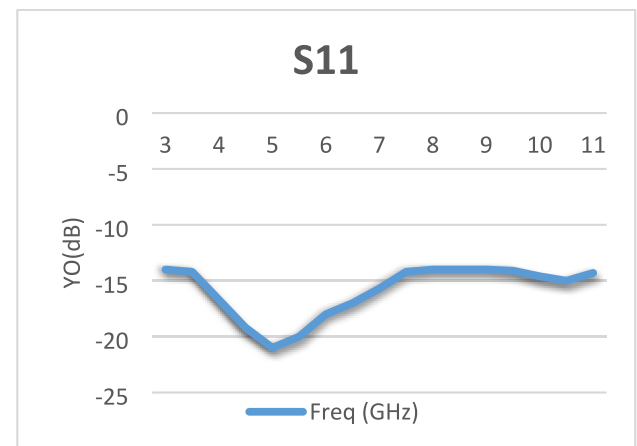


Fig. 17 Matching property of the post-layout of the proposed LNA

$$\begin{aligned} |I_{n,out,M1}| &= |I_{n,M1}| \frac{(sC_2 \bullet E + BE(1 - A) \bullet g_m)}{(sC_2 \bullet E + BE(1 - A) \bullet g_m)} \\ &\bullet \frac{1}{(1 - D \bullet sC_2)} \end{aligned} \quad (39)$$

Therefore, the total noise of the proposed LNA due to (26) and (39) can be sated as:

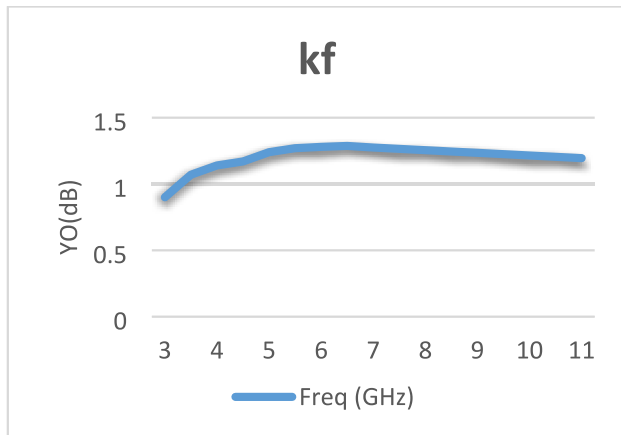


Fig. 18 Stability factor of the post-layout of the proposed LNA

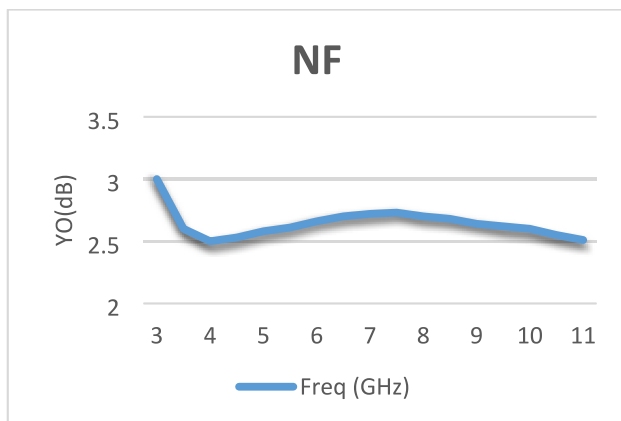


Fig. 19 NF result of post-layout of the proposed LNA

$$NF = 1 + \frac{\gamma g_m}{4R_s} \left(\frac{1}{(1 - D \bullet sC_2)} \right)^2 \cdot \frac{(1 - D \bullet sC_2)}{(sC_2 \bullet E + BE(1 - A) \bullet g_m)} \quad (40)$$

3.4 IIP3 Analysis

In this section, linearity and IIP3 analysis is performed using Volterra series. Considering second and third harmonic signals of Fig. 6, we have:

$$i_{ds} = g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 + \dots \quad (41)$$

The large signal trans-conductance of transistor can be calculated as:

$$G_m = g_m + \frac{\partial g_m}{\partial V_{gs}} V_{gs} + \frac{1}{2} \frac{\partial^2 g_m}{\partial V_{gs}^2} V_{gs}^2 + \dots \quad (42)$$

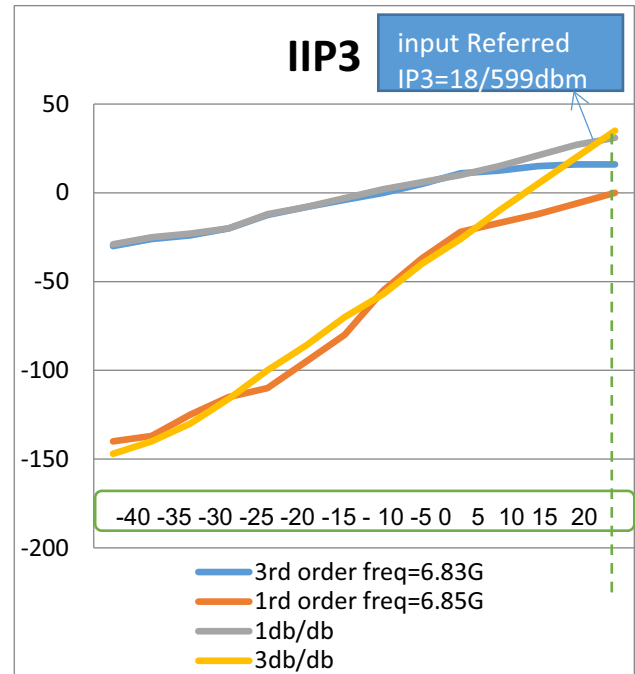


Fig. 20 IIP3 result of post-layout of the proposed LNA

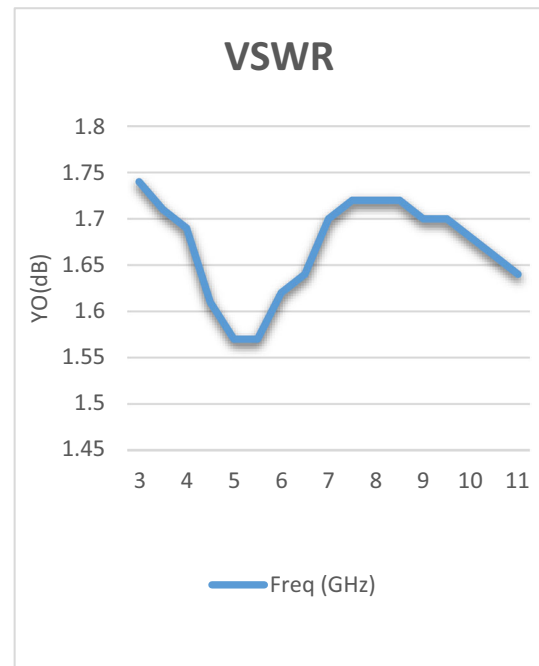
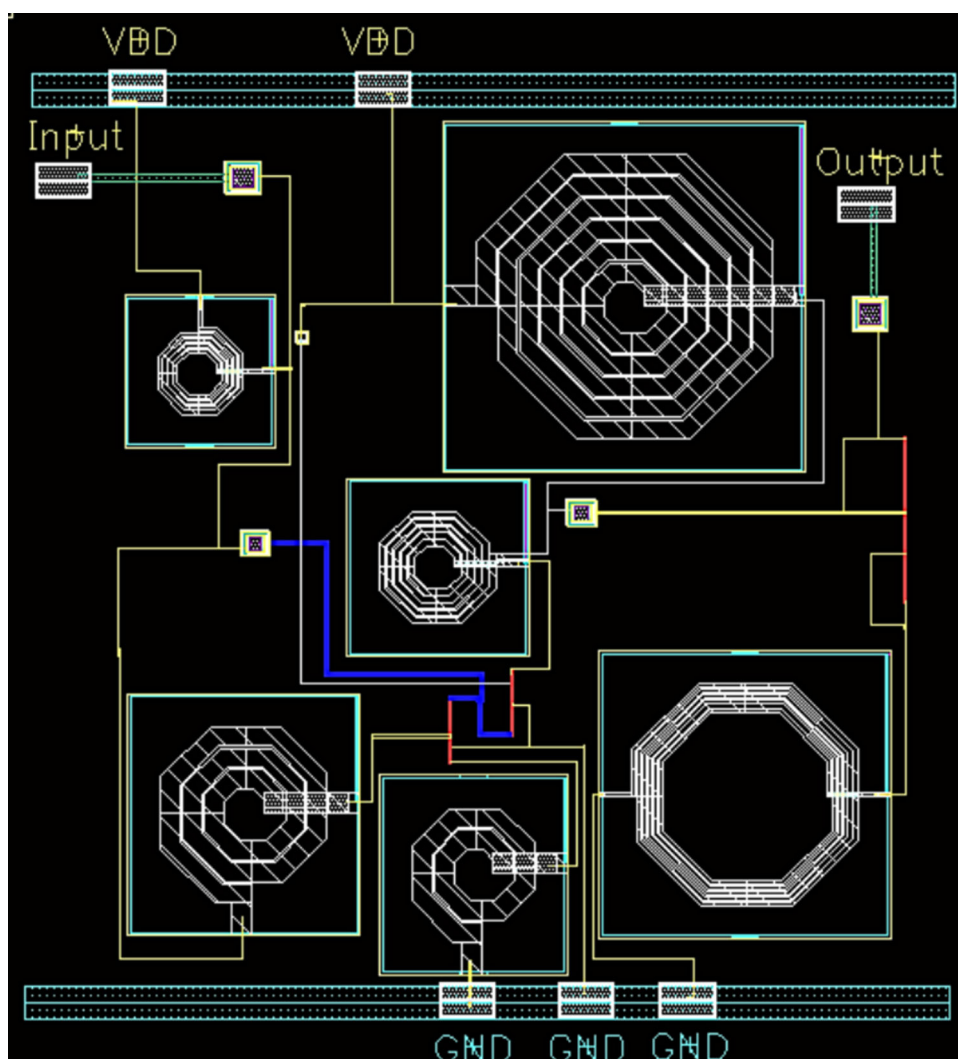


Fig. 21 VSWR result of post-layout of the proposed LNA

In consequence, two in-band signals with equal amplitude and two different frequencies are applied to the proposed circuit and we have:

$$v_1(t) = \frac{V_{gs}}{2} (e^{j\omega_1 t} + e^{-j\omega_1 t})$$

Fig. 22 Layout the proposed LNA



$$v_2(t) = \frac{V_{gs}}{2} (e^{j\omega_2 t} + e^{-j\omega_2 t}) \quad (43)$$

Then, the drain current can be stated as:

$$i_d(t) = G_m(v_1(t) + v_2(t)) \quad (44)$$

Using (42) and (43) in (44) and after some simplifications, we finally have:

$$\begin{aligned} i_d(t) = & \frac{g_m V_{gs}}{2} (e^{j\omega_1 t} + e^{-j\omega_1 t} + e^{j\omega_2 t} + e^{-j\omega_2 t}) \\ & + \frac{3}{16} \frac{\partial^2 g_m}{\partial V_{gs}^2} V_{gs}^3 (e^{j(2\omega_1 - \omega_2)t} + e^{-j(2\omega_1 - \omega_2)t} \\ & + e^{j(2\omega_2 - \omega_1)t} + e^{-j(2\omega_2 - \omega_1)t}) \end{aligned} \quad (45)$$

Thus, the power of desired signal can be presented as:

$$P_{main} = \frac{g_m^2 V_{gs}^2}{2} R_L \quad (46)$$

and the power of third-harmonic signal is obtained as:

$$P_{IM3} = \frac{9}{64} \left(\frac{\partial^2 g_m}{\partial V_{gs}^2} \right)^2 V_{gs}^6 R_L \quad (47)$$

Using the proposed structure and PD method in the second stage, the parameter of P_{IM3} (gm_3) is reduced and therefore, the linearity range is extended leading to the increasing of the IIP3.

4 Results and Discussion

4.1 Simulation Results

The performance of the proposed LNA is discussed in this section focusing on the simulated circuit. Simulation is done with ADS software where the gain analysis simulation is described by the parameter S_{21} depicted in Fig. 10. As can be seen, the gain is high and almost smooth in the desired bandwidth. S_{11} is presented to show the matching

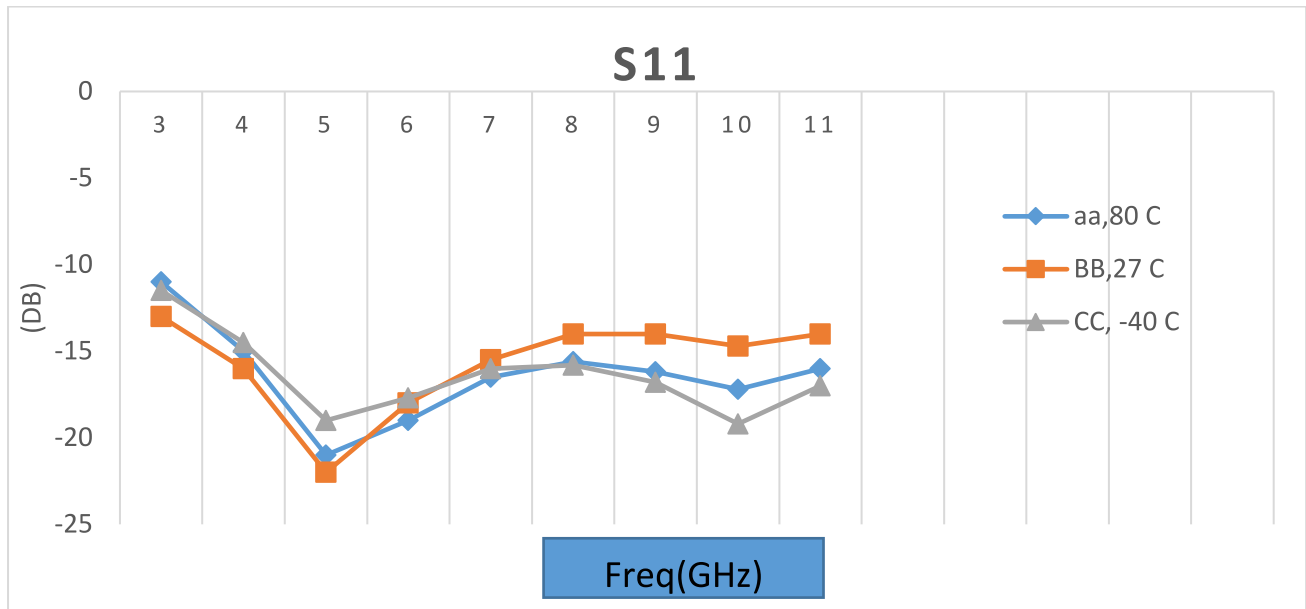


Fig. 23 Input matching property of post-layout result in three different temperatures (27, 80 and -40)

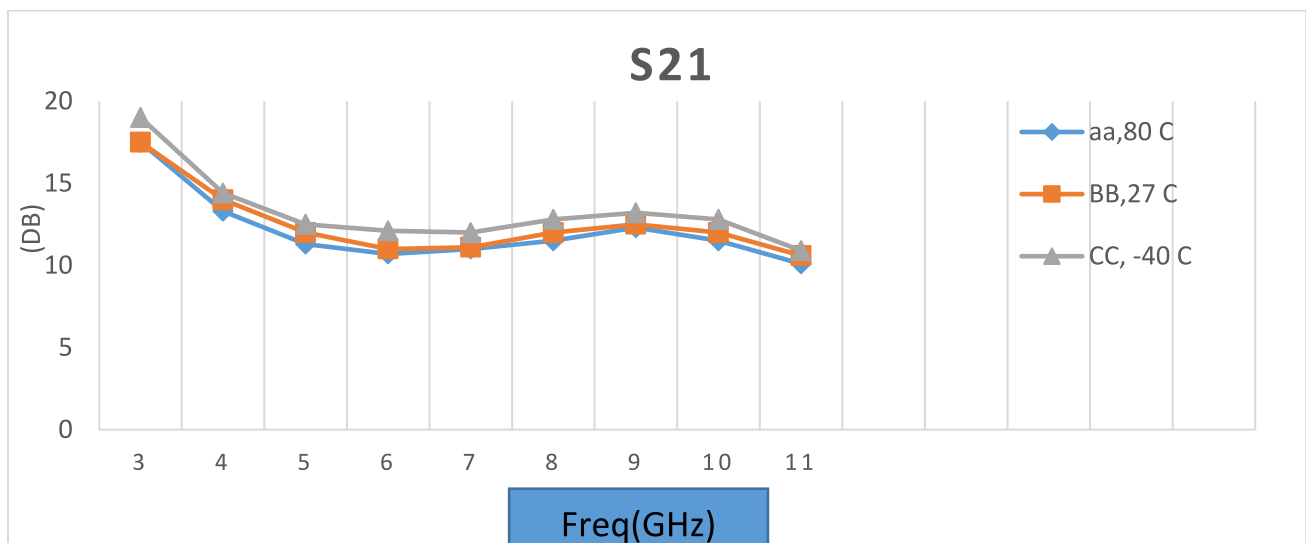


Fig. 24 Gain result of post-layout in three different temperatures (27, 80 and -40)

property of the proposed structure which is desirably less than -10 dB as observable from Fig. 11. The stability of the proposed LNA is tested and shown in Fig. 12 which is higher than 1 in the designed bandwidth. The noise figure result is depicted in Fig. 13 which is lower than 3 dB. This NF is notable in the designed bandwidth. To measure the linearity and IIP3, two-tone test is used, where two signals with different frequencies and equal powers are applied while the power of the input signal is gradually increased. Figure 14 shows the resulted IIP3 as 18.599 dBm which is desirable. Figure 15 also shows the VSWR parameter of the proposed LNA which denotes the

matching property of the circuit. The value of VSWR is between 1 and 1.5 which verifies the matching design procedure.

4.2 Post-Layout Results

To verify the simulation results of the previous section, layout of the proposed structure must be generated using the CADENCE and the post-layout results must be compared to the simulation results. Obviously, both results must follow each other to achieve the final confirmed and efficient circuit. The post-layout test results are done in

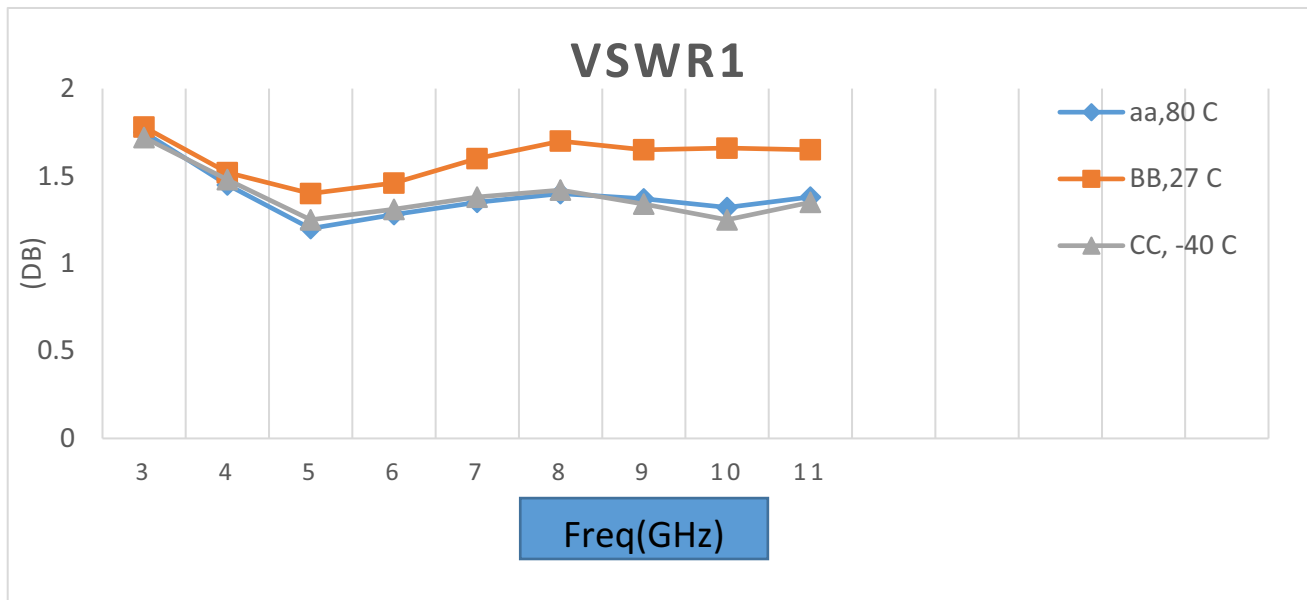


Fig. 25 VSWR of post-layout result in three different temperatures (27, 80 and -40)

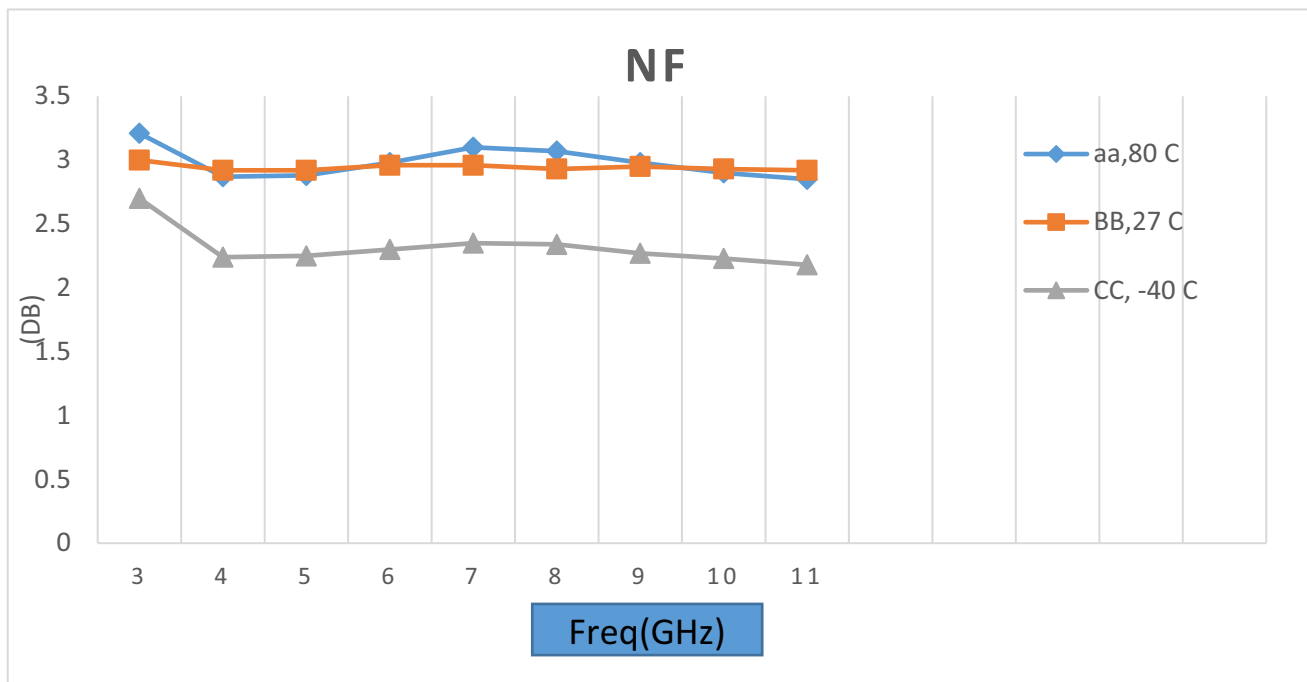


Fig. 26 NF of post-layout result in three different temperatures (27, 80 and -40)

three different temperatures to obtain different operation modes of the proposed structure and also the robustness of the LNA in these states. Similar to the previous section, firstly the gain and matching property are tested and presented in Figs. 16 and 17, respectively. As can be seen from these figures and comparing with the related figures of the previous section, the results verify each other in both sections. In addition, the corresponding parameters

such as stability factor, NF, IIP3 and VSWR are also shown in Figs. 18, 19, 20 and 21, respectively. All figures verify the related figures of the previous section as can be compared.

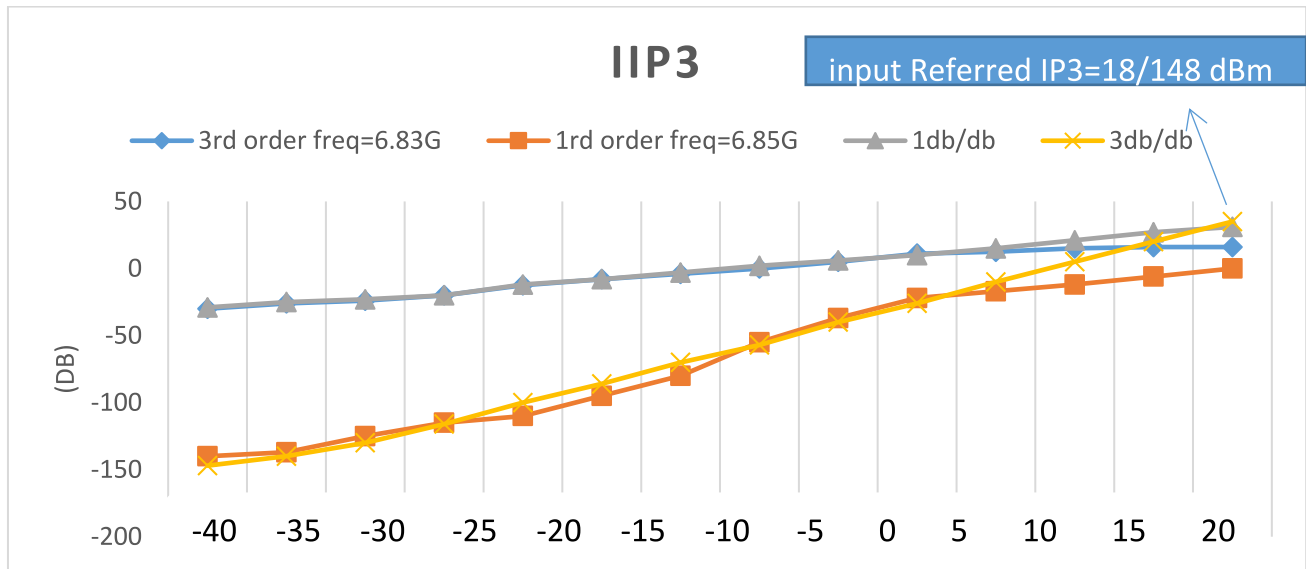


Fig. 27 IIP3 property of post-layout result in the temperature -40

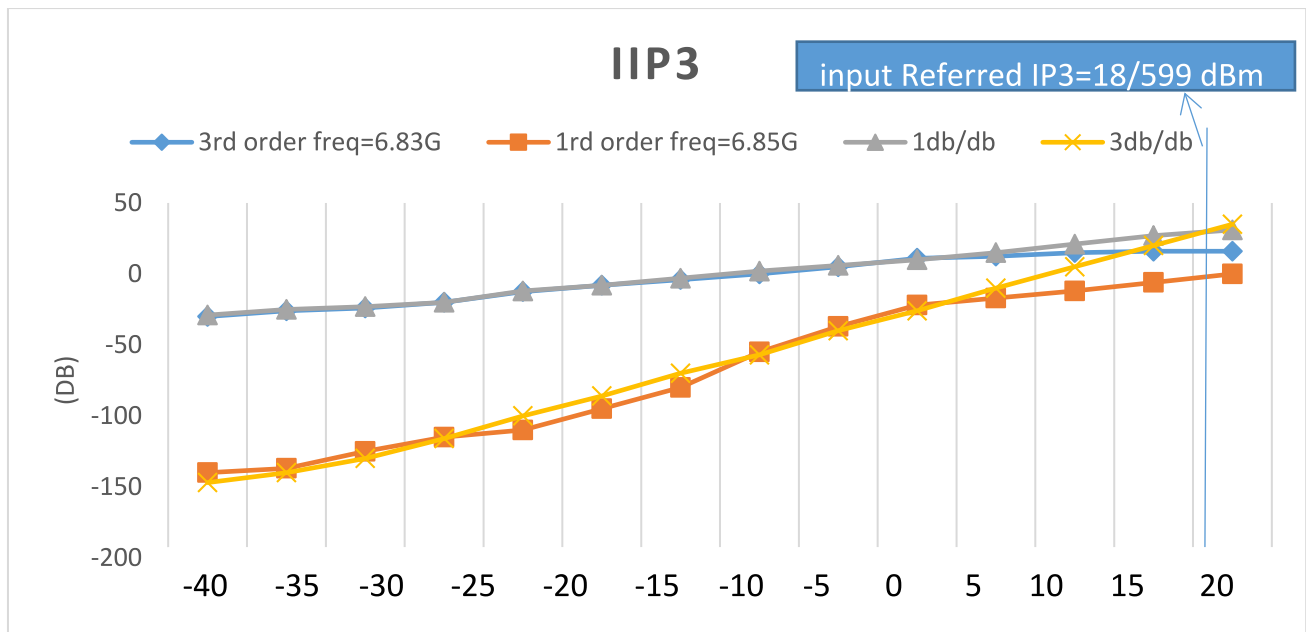


Fig. 28 IIP3 property of post-layout result in the temperature 27

4.3 Power Consumption

Power consumption is one of the main properties of each LNA. In the proposed circuit, the current drawn from the voltage source of 1.2 V is equal to 12.9 mA, which leads to the power loss of 15.5 mW. This power consumption is acceptable to achieve the linearity range extension compared to other efficient structures in the literature (comparison table is presented in the next section).

4.4 Post-Layout Results in Temperature Analysis

The final layout structure of the proposed LNA is shown in Fig. 22 which can be fabricated in 180-nm technology. In the consequence, the temperature analysis of the post-layout circuit is done to show the performance of the proposed structure in different temperature conditions.

For temperature analysis, three different temperatures as 27, 80 and -40 (degree-Celsius) are investigated in the CADENCE environment where the performance results are assessed. This analysis shows the design stability in

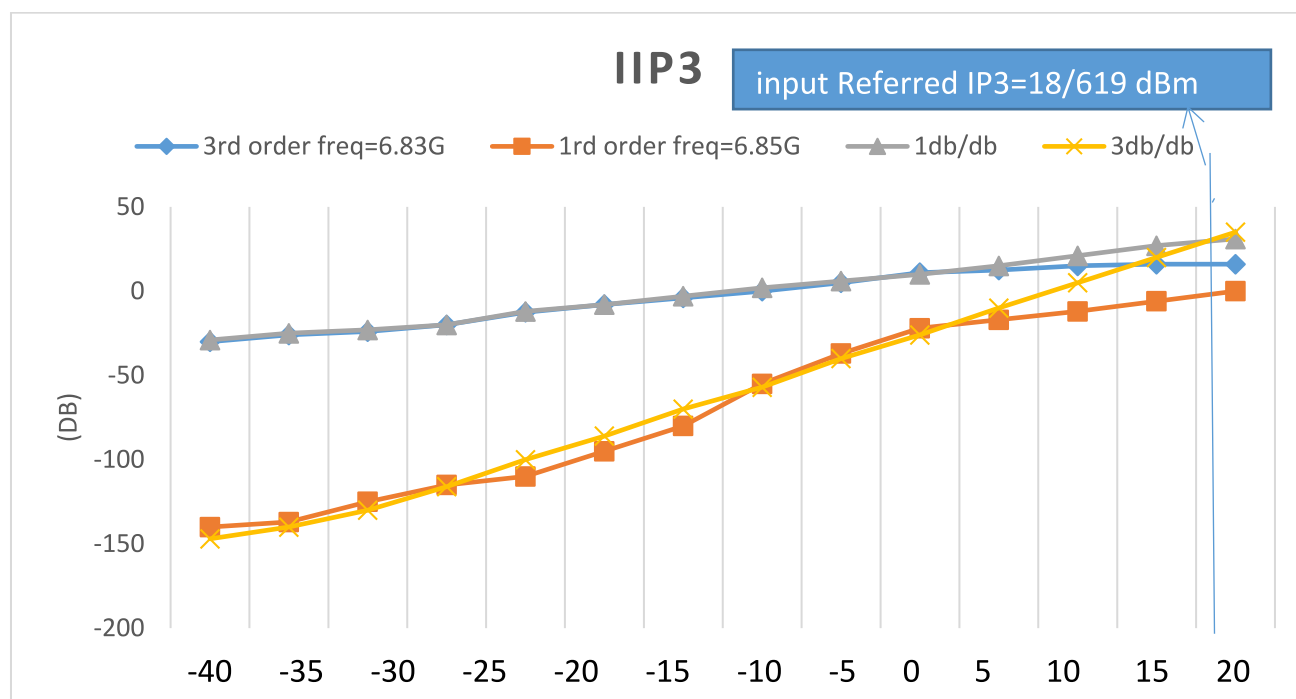


Fig. 29 IIP3 property of post-layout result in the temperature 80

Table 2 Comparison of the proposed LNA with other efficient works

Technology μm	FOM	Power mW	S_{11} dB	IIP3 dBm	NF dB	S_{21} dB	BW GHz	Reference
0.18	11.12	15.5	-13.35	18.59	2.4–2.8	11.125	3.1–10.6	Proposed work
0.15	2.8	96	10-	12.1	1.9–2.4	20	27–35	Yousef et al. 2014)
0.18	7.36	8.96	-18.3	7.36	2.17–3.4	13–17.5	0.8–1.2	Seng-Woon and Maas 2009)
0.32	1.74	8.05	7.5-	-10	2.8	22.8	3.1–10.6	Yaghouti and Yavandhasani 2021a)
0.09	5.35	11.2	10-	13.8	1.8–4	12.6	0.1–7	Li, et al. 2020)
0.65	2.78	16	8.7-	-5.7	3	15.6	3–10	Pandey and Singh 2015)
0.18	3.32	1.3	-9	-1	3.5	12.25	5	Guo et al. 2017)
0.18	4.69	28.44	-10.7	20	2.4	9.34	5.8	Yaghouti and Yavandhasani 2021b)
0.18	3.07	6	10-	3.84	2.5–4	0.5 ± 10.8	3.1–10.6	Singh et al. 2018)
0.13	3.12	10.6	-20	12.6	5.8	12.6	1.6–9.7	Rafati et al. 2019)
0.18	3.76	11	-11	-4	3.34–4.62	13.58	3–12	Reddy and Sravani 2017)
0.18	4.2	3.8	-8.5	-10.5	3.6	9	2.8–7.5	Daryabari et al. 2019c)

different temperature conditions. Figure 23 shows the input matching property in term of the temperature analysis which denotes the notable performance of matching of the proposed LNA in all temperatures. Similar analysis is done for other parameters such as gain, VSWR and NF in Figs. 24, 25 and 26, respectively. Moreover, the analysis of the linearity (IIP3) is accurately performed in different temperatures which are shown in Figs. 27, 28 and 29 for

temperatures -40, 27 and 80, respectively. Because of design focus on the linearity improvement, three figures are separated for three temperatures. As can be seen from these figures, due to the proper designed structure, the performance of the proposed LNA is not degraded in different temperatures where it maintains the desirable performance in different conditions.



As the final assessment, the comparison of the proposed LNA with other efficient LNA structures in the literature is described in Table 2. As can be understood from this table, different quality parameters such as bandwidth, matching, NF and IIP3 are compared where the global parameter as figure of merit (FOM) is also mentioned which is defined as (Benqing Guo and Xiaoleili 2013; Luo et al. 2019; Lin et al. 2022):

$$FOM = \frac{GAIN(dB) \bullet IIP3}{(NF - 1)POWER(mw)} \quad (48)$$

From this table, the notable performance of the proposed structure in terms of NF and IIP3 can be observed. Thus, the proposed design is efficient to be applied in the wireless communication receivers.

5 Conclusion

The proposed LNA of this paper has notable properties based on power derivative method and cascode structure. The main focus of the design is on the linearity extension as the IIP3 is achieved as 18.599 dBm. NF is 2.6 dB which is desirable in the bandwidth of 3.1–10.6 GHz. In addition, these improvements are obtained with power consumption of 15.5 mW which is desirably low and suitable for wireless communication receivers. Moreover, the final size of the structure is small enough to be integrated in high-technology circuits.

For future works, an efficient LNA in other frequencies can be considered where other parameters such as lower power consumption and higher gain can be mainly focused. In addition, other scalings such as 130-nm technology can be presented and tested to achieve more efficient LNA.

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