

A 24-27 GHz wideband LNA in 40nm RF CMOS Technology

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Abstract- In this paper, a single-ended wideband low noise amplifier (LNA) in the *K*-band is presented. By utilizing a two-stage common-source (CS-CS cascode) current reuse topology, the LNA circuit achieves low power consumption and low return loss. By adding another transistor as a third stage to amplify the signal, the LNA can further increase the gain while maintaining linearity. Implemented using a standard 40nm RF CMOS process, the proposed LNA demonstrates more than 12 dB gain and less than 5.1 dB noise figure across the 24 GHz to 27 GHz band, with input and output return loss below -15 dB.

Index CS-CS-cascode, current reuse, *K*-band, LNA, RF CMOS

I INTRODUCTION

Low-noise amplifier (LNA), as the first active circuit in radio frequency (RF) front-end, is a key device that impacts two critical performance indicators of a RF system: sensitivity and dynamic range. For 5G millimeter-wave communication, the *K*-band is attractive due to its wide frequency band available for digital data transmission. Although CMOS technology offers low cost, high integration, and low power consumption opportunities, RF circuit design in CMOS still involves power consumption concerns due to the inherent low transconductance of MOSFET [1]. In addition, traditional CMOS limits DC supply voltage, therefore, maintaining sufficient overdrive voltage is one of the design challenges.

The LNA power consumption may be reduced through two ways: one is to reduce the supply voltage, such as gate bias technology; and the other is to reduce the circuit total current, such as current reuse technology. The basic current-reuse structure is composed of two common-source (CS) MOSFET transistors. The two transistors share the same DC bias current, so that the power consumption is halved as compared with the cascaded topology, but the circuit transconductance is still the product of the individual transconductances of the two transistors. Therefore, the final power gain is as high as the cascaded topology. Besides low power consumption, current reuse technology also uses fewer inductors, making the LNA be compact.

II CIRCUIT DESIGN

The LNA schematic is shown in Fig. 1, which is based on a two-stage CS-CS cascoded current-reuse structure. The third stage is cascaded with a CS MOSFET to obtain high gain.

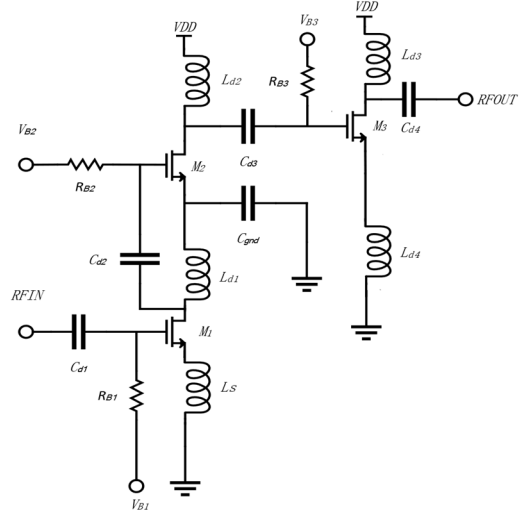


Fig. 1. Schematic diagram of the proposed LNA.

Resistors R_{B1} , R_{B2} , and R_{B3} with large resistance are used as RF choke, while providing bias voltage V_{B1} , V_{B2} , and V_{B3} for the transistors. In static state, transistors M_1 and M_2 share the DC bias current flowing through L_{d1} . During AC operation, the amplified RF signal from M_1 is blocked by the high impedance of L_{d1} and flows to M_2 through the coupling capacitor C_{d2} . Therefore, the overall transconductance of the circuit equals to the product of the individual transconductances of M_1 and M_2 , thus achieving two-stage amplification using the same single bias current, which enables low-power consumption [2]. C_{d1} and C_{d4} are DC block capacitor, C_{gnd} is an AC bypass capacitor to the ground, and L_{d3} and C_{d4} compose an output matching network to provide broadband impedance matching.

The inductance L_S and the gate-source capacitance C_{gs} form a resonance at frequency ω_0 :

$$\omega_0 = \frac{1}{\sqrt{C_{gs} \cdot L_S}} \quad (1)$$

Changing the L_S value affects the Q value of the matching network as well as the resonance frequency, as shown in Fig. 2. It should be noted that an excessively large L_S leads to significant reduction in gain. Therefore, the value of L_S should be carefully selected.

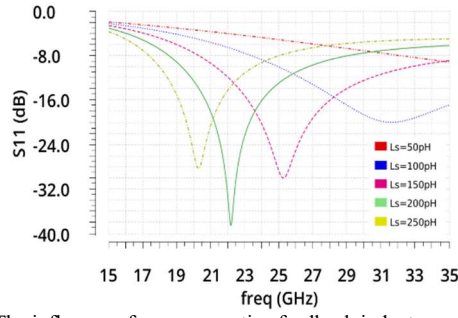


Fig. 2. The influence of source negative feedback inductance L_S on S_{11} .

III SIMULATION AND MEASUREMENT RESULTS

The LNA is designed using a 40nm RF CMOS process. The LNA layout is given in Fig. 3, which is 0.472mm*0.391mm in size and 0.19mm² in total area, demonstrating the chip area advantage of the current LNA structure.

Post-layout simulation is carried out by using EM simulation tool EMX for key metal pieces in the design. The plots below are all based on post-layout simulation.

The single-ended wideband LNA features a small signal gain of 12 dB over 24-27 GHz, with an in-band flatness of less than 1 dB, and input and output return loss are less than -15 dB, as illustrated in Fig. 4. The LNA noise figure is less than 5.1 dB and the stability factor Kf remains above 8 throughout the frequency band as shown in Fig. 5 (a).

The 1dB gain compression point ($IP1dB$) is also simulated. At 25.5 GHz, an $IP1dB$ of -7.37dBm is obtained as shown in Fig.5 (b) which is better than the results reported in most literature.

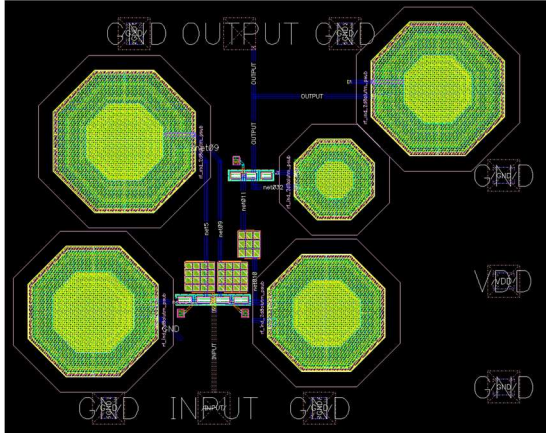


Fig. 3. Layout of LNA design.

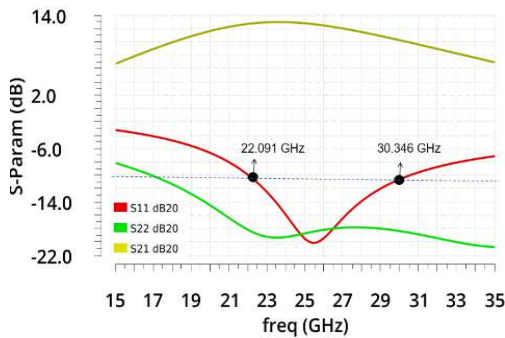


Fig. 4. Measured S_{11} , S_{21} and S_{22} of the LNA.

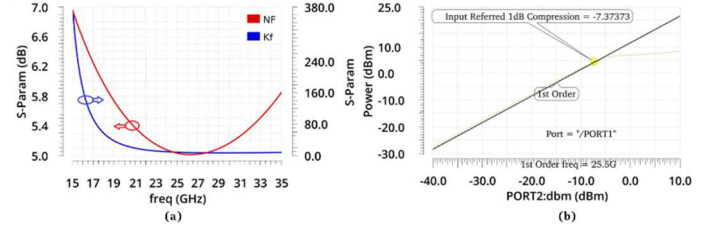


Fig. 5.(a) Measured NF and Kf of the LNA. (b) Measured Input Referred 1dB Compression.

TABLE I
PERFORMANCE SUMMARIES AND COMPARISONS WITH RECENTLY REPORTED CMOS LNAs

Reference	This work	[3]	[4]	[5]
Process	40nm	22nm	40nm	0.13um
Supply(V)	1.1	0.8	-	1.5
Frequency(GHz)	24-27	24-28	24-40	24
Gain(dB)	12	14.7	23	31.2
NF(dB)	5.1	3.15	3.7	4.9
$IP1dB$ (dBm)	-7.37	-12	-15.9	-
Area(mm ²)	0.19	0.26	0.22	0.53

Finally, TABLE I summaries the performance of the current LNA design and compares it with previously published works [3]-[5]. Our LNA is the most compact one. Using S_{11} , $S_{22} < -10$ dB as criteria, the bandwidth of our LNA is roughly from 22GHz to 30 GHz.

IV CONCLUSION

This paper presents a 24-27 GHz 3-stage common-source LNA implemented using 40nm RF CMOS technology, targeting for millimeter-wave 5G applications. The design utilizes a current-reuse structure at the input and compensates for gain using an LC parallel resonant feedback network. Post-layout simulation demonstrates a gain of 12dB, with smooth gain response and input and output loss below -15dB. The noise figure is less than 5.1dB across the operating frequency range. The linearity is -7.6 at 25.5 GHz. The total power consumption is 35.5mW which will be further reduced in future work.

REFERENCES

- [1] Wang, Y. S. , and L. H. Lu . "5.7 GHz low-power variable-gain LNA in 0.18 μ m CMOS." Electronics Letters 41.2(2005):66-68.
- [2] M. -D. Wei, S. -F. Chang and Y. -C. Liu, "A Low-Power Ultra-Compact CMOS LNA with Shunt-Resonating Current-Reused Topology," 2008 European Microwave Integrated Circuit Conference, Amsterdam, Netherlands, 2008, pp. 350-353.
- [3] S. George, M. Cui and P. Sen, "A 24-28 GHz Tunable LNA in 22nm FDSOI Technology," 2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Istanbul, Turkiye, 2023, pp. 1-4.
- [4] C. Fang, Q. Wu, H. Wang and W. Hong, "A 24-40 GHz Wideband LNA with Gain Compensation in 40-nm CMOS for 5G Applications," 2023 16th UK-Europe-China Workshop on Millimetre Waves and Terahertz Technologies (UCMMT), Guangzhou, China, 2023, pp. 1-3.
- [5] Z. Cao et al., "A K-Band High-Gain LNA in 0.13- μ m RF CMOS," 2019 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Nanjing, China, 2019, pp. 1-3.