

Design of a Dual-Band LNA With Dual-Band Complex Load Impedance Transformer and Noise-Cancelling Technology

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Abstract—In this paper, a dual-band low-noise amplifier (DB-LNA) operating in the Ku band is proposed. This DB-LNA combines dual-band complex load impedance transformer and noise-cancelling (NC) technology. A multi-section microstrip line is used to achieve the input, interstage and output matching. To reduce the noise figure (NF) of the DB-LNA, the NC technology is used, which generates an inverse signal to cancel out the noise. The proposed LNA, designed in a 0.1- μm InGaAs process, demonstrates excellent performance at the two operating bands. The simulation results show the peak gain of 27.8dB and 25.4dB, the minimum NF of 1.33dB and 1.29dB, and the input third-order intercept point (IIP3) of -8dBm and -4.5dBm at 12.9GHz and 17.1GHz.

Index Terms—dual-band low noise amplifier, dual-band complex load impedance matching, noise-cancelling technology.

I. INTRODUCTION

In the present age of uninterrupted technological advancement, there is a growing need for wireless communication equipment. As a crucial component of RF receivers, the low-noise amplifiers (LNAs) receive a multitude of intricate signals from diverse frequency bands.

A number of possible ways to work at dual-frequency band have been proposed. The initial approach is to implement dual-frequency band by paralleling two single-band bands [1]. But this way results in extremely high-power consumption and chip area. In order to solve the problem of power consumption, the use of switched inductors or switched capacitors is proposed [2]. Although the power consumption problem is solved, it can only switch between two frequency band. Another solution is to use a wideband low-noise amplifier including the two required frequency band, and introduce a band-reject filter to filter out the unwanted frequency band [3]. Zhengmin Ke proposes an ultra-low noise parallel DB-LNA based on a substrate integrated suspension line (SISL) platform, which greatly improves noise and gain performance [4]. Various techniques adopted by the DB-LNAs are described in [9][10][11], and their excellent performance is demonstrated.

In this paper, the design of a two-stage DB-LNA utilizing 0.1- μm InGaAs process is presented. The article provides a concise overview of the frequency-dependent dual-band complex load impedance transformer and NC technology, as well as the simplified schematic of the proposed DB-LNA. Finally, a summary and comparison of the simulation results are presented.

II. THEORY AND STRUCTURE OF CIRCUIT

A. Dual-Band Complex Load Impedance Matching transformer

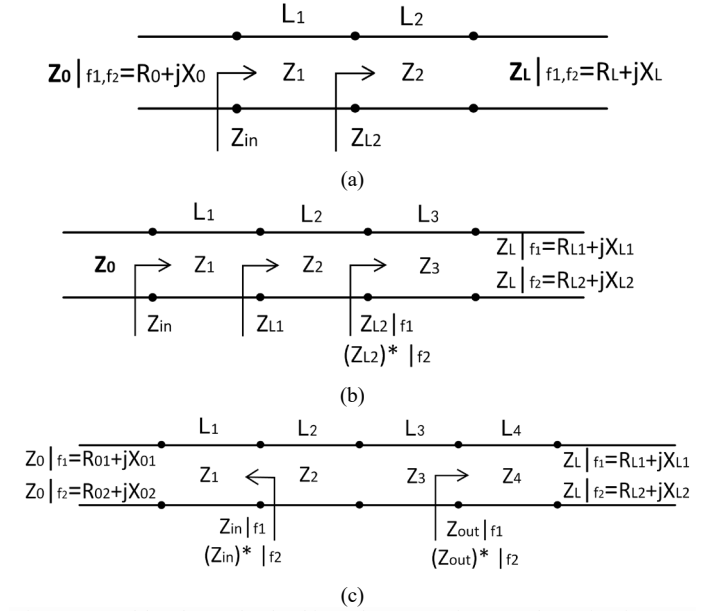


Figure 1. Dual-band complex load impedance transformer Schematic of (a) two-stage, (b) three-stage, (c) four-stage.

A dual-band frequency-dependent complex load impedance matching network is proposed, building upon the traditional two-stage dual-band impedance transformer shown in Figure 1(a). Previous work in [6] has placed restrictions on input and load impedance by assuming a frequency-independent complex impedance, which presents a challenge in matching frequency-dependent complex impedance. To address this issue, a three-stage dual-band impedance transformer was introduced in [7], shown in Figure 1(b), which utilized the third microstrip line to convert any frequency-dependent complex load impedance at two frequency points into a pair of complex conjugate impedances. The remaining two sections of the transformer, similar to Figure 1(a), achieved frequency-independent complex impedance matching with the real impedance under the dual band.

However, the three-stage dual-band impedance matching network could not solve the simultaneous matching of two frequency-dependent complex load impedances of input and output at the dual-frequency point in actual condition.

Therefore, a four-stage dual-frequency transformer was proposed in [8]. Building on the theory presented in [7], the addition of one microstrip line converted the arbitrary complex load impedance at the other end into a pair of complex conjugate impedances, as shown in Figure 1(c).

A three-stage dual-band complex load impedance transformer is shown in Figure 1(b). By adding Z_3 , Z_{L2} at the two operating frequencies is as follows:

If $Z_{L2}|_{f_1} = Z_{L2}|_{f_2}$, the remaining two-stage impedance matching network is solved directly according to the two-stage complex load impedance transformer [6].

If $Z_{L2}|_{f_1} = (Z_{L2}|_{f_2})^*$, The relevant parameters can be obtained through the following process. First, we use Z_3 to match Z_L and Z_{L2} , and Z_{L2} at the two frequencies are respectively:

$$Z_{L2}|_{f_1} = Z_3 \frac{R_{L1} + jX_{L1} + jZ_3 \tan(\beta_1 l_3)}{Z_3 + j(R_{L1} + jX_{L1}) \tan(\beta_1 l_3)} \quad (1a)$$

$$Z_{L2}|_{f_2} = Z_3 \frac{R_{L2} + jX_{L2} + jZ_3 \tan(\beta_2 l_3)}{Z_3 + j(R_{L2} + jX_{L2}) \tan(\beta_2 l_3)} \quad (1b)$$

Here, Z_L represent a compromise between noise and gain at two center frequencies. according to the conjugate relationship in the (1a) and (1b), a series of simplifications can be performed to obtain:

$$Z_3 = \sqrt{R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1} + X_{L2}}{R_{L2} - R_{L1}} (R_{L1}X_{L2} - R_{L2}X_{L1})} \quad (2)$$

$$l_3 = \frac{n\pi + \arctan \frac{Z_3(R_{L1} - R_{L2})}{R_{L1}X_{L2} - R_{L2}X_{L1}}}{(m+1)\beta_1} \quad (3)$$

Assuming $f_1 < f_2$, then $\frac{f_2}{f_1} = m, m > 1$. Here n can be any integer, but in order to minimize L_3 and reduce the footprint of the layout, one or zero is generally chosen.

Once Z_3, L_3 is settled, it becomes a two-stage complex load impedance matching from Z_0 to Z_{L2} :

$$Z_{L1} = Z_2 \frac{Z_{L2} + jZ_2 \tan(\beta l_2)}{Z_2 + jZ_{L2} \tan(\beta l_2)} \quad (4)$$

$$Z_{in} = Z_1 \frac{Z_{L1} + jZ_1 \tan(\beta l_1)}{Z_1 + jZ_{L1} \tan(\beta l_1)} \quad (5)$$

Because the input and output impedances are 50Ω , the Z_{in} is matched to 50Ω here. since each expression corresponds to two frequency points, the transcendental equation of four variables is generated. Z_1, Z_2, L_1, L_2 can be obtained by combining numerical methods and optimization algorithms. The four-stage method is similar to the three-stage method and is not described in detail here.

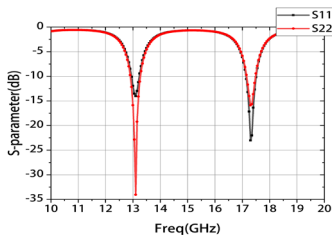


Figure 2. Simulated S-parameters of three-stage dual-band transformer.

From Figure 2, it can be observed that the three-stage transformer matches well at both required frequencies, with a 10 dB return loss bandwidth exceeding 300 MHz for each frequency band. This demonstrates the effectiveness of the proposed solution.

B. Noise-Cancelling Technology

The above DB-LNA based on the frequency-dependent dual-band complex load impedance matching technique fails to deliver satisfactory noise performance. Therefore, the NC technology is introduced by cascading a common source transistor M2 at the input of the common source transistor M1. This transistor acts as an auxiliary amplifier and generates a noise with opposite phase as the main amplifier. Then the two signals are superimposed using a source follower M3 to cancel the noise and harmonics of the main amplifier [5].

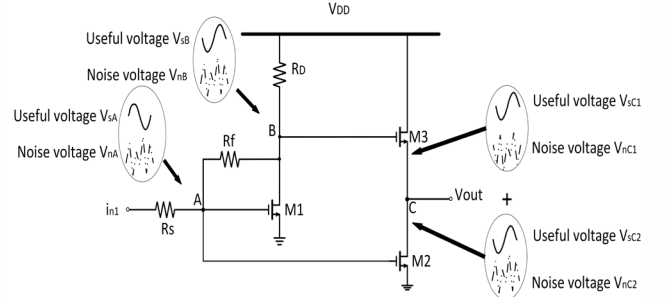


Figure 3. LNA based on noise-cancelling technology.

The basic structure of LNA that employs the NC technology is shown in Figure 3. At the signal input terminal V_{in} , there exists a current i_{n1} . When i_{n1} flows through R_s and R_f , it produces noise voltages V_{nA} and V_{nB} at nodes A and B, respectively, both having the same polarity. The useful voltage V_{sA} at node A is amplified by M1, producing the polarity-reversed V_{sB} at node B. Subsequently, the polarity of the useful voltage V_{sB} and the noise voltage V_{nB} at node B remain unchanged after passing through the source follower M3, becoming the useful voltage V_{sC1} and the noise voltage V_{nC1} . Furthermore, the useful voltage V_{sA} and the noise voltage V_{nA} are amplified by M2, producing the polarity-reversed useful voltage V_{sC2} and the noise voltage V_{nC2} at node C. Therefore, the noise voltage at node C is canceled out, while the useful voltage is added. The relevant derivation process is as follows:

The noise voltages flowing through nodes A and B is:

$$v_{n,A} = i_{n1} \times R_s \quad (6a)$$

$$v_{n,B} = i_{n1} \times (R_s + R_f) \quad (6b)$$

Combined (6a) and (6b) can be obtained:

$$\frac{v_{n,B}}{v_{n,A}} = 1 + \frac{R_f}{R_s} \quad (7)$$

The gain through amplifiers M_2 and M_3 is denoted as A:

$$A = -\frac{g_{m2}}{g_{m3}} \quad (8)$$

So, when $-A = 1 + \frac{R_f}{R_s}$, complete cancellation of noise can theoretically be achieved.

C. DB-LNA Architecture

The DB-LNA designed in this article, as shown in Figure 4, adopts the cascaded multi-section microstrip line to achieve dual-band impedance matching, which is relatively simple to implement. In order to meet the low NF requirements, the NC technology is used here. By introducing an auxiliary transistor to cancel the noise in the main path and superimposing the useful signal to increase the gain. However, generally, the single-stage gain is not high enough, so this design uses a two-stage amplification structure to increase the gain. The entire circuit consists of a two-stage LNA that use the NC and source follower feedback technology, as well as input, output and inter-stage dual-band matching networks.

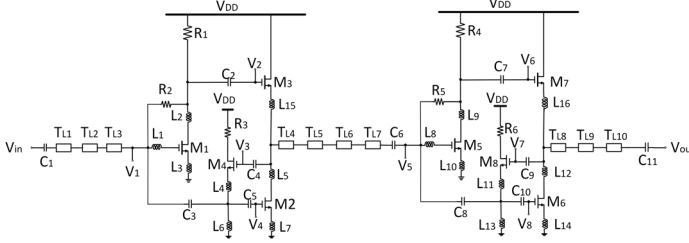


Figure 4. Simplified schematic of the proposed DB-LNA.

III. SIMULATION RESULT

The following figures are the result of simulation and optimization using ADS2019. It can be seen that the designed DB-LNA achieves great gain and noise performance around 12.9/17.1 GHz frequency points.

Figure 5(a) show the magnitudes of the S-parameters at 12.9 and 17.1 GHz are -18.35 and -20.6 dB for S11, -12.29 and -16.35 dB for S22, respectively. Figure 5(b) displays the noise figure (NF) and gain simulation results, with the NF values of 1.33 dB and 1.29 dB at 12.9 and 17.1 GHz, and gains of 27.8 and 25.4 dB at these two frequencies. The IP_{1dB} and IIP3 are shown in Figure 6, with the IP_{1dB} values of -27 and -25 dBm at 12.9 and 17.1 GHz, respectively, and the IIP3 values of -8 and -4.5 dBm at these two frequencies.

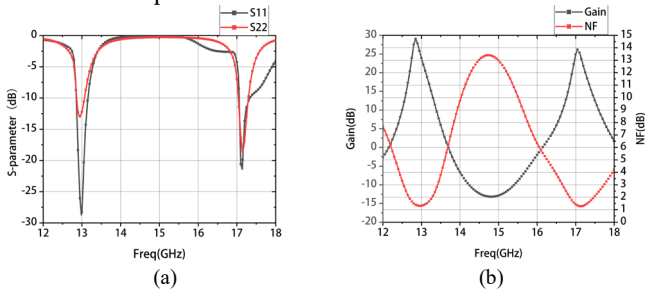


Figure 5. Simulated of (a) S11 and S22. (b) Gain and NF.

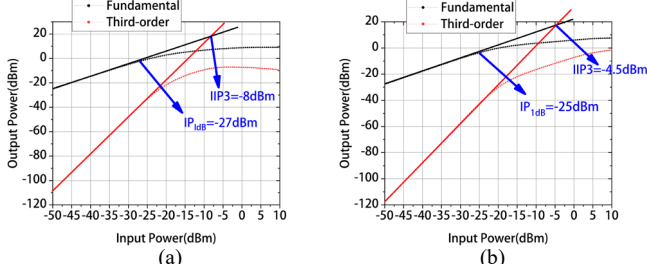


Figure 6. Simulated IP_{1dB} and IIP3 at (a) 12.9GHz. (b) 17.1GHz.

TABLE I PERFORMANCE SUMMARY AND COMPARISON

Reference	Frequency (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)
[4]	2.45	0.7	28.4	-6.6
	5.25	1.1	28.8	-5.1
[9]	10	5.3	25.35	N/A
	24	10.4	12.12	N/A
[10]	26-30	3.84	13.68	-7.15
	37-40	4.47	13.04	-6.85
[11]	28	3.1	18.1	N/A
	39	3.8	18.4	N/A
This work	12.9	1.33	27.8	-8
	17.1	1.29	25.4	-4.5

A comparison of the proposed DB-LNA with other DB-LNAs is summarized in Table I. The results show that the NF of the proposed DB-LNA is lower than that of others, and that it achieves high peak gain.

IV. CONCLUSION

The present paper proposes a two-stage cascaded DB-LNA based 0.1- μ m InGaAs process. To achieve great matching and low noise at both operating frequencies, frequency-dependent dual-frequency complex impedance transformer and NC technology are employed. The proposed DB-LNA demonstrates a gain exceeding 20dB, the NF below 2dB, and prominent selectivity at both frequencies.

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