



Analysis of the Impact of the Inductive Peaking Bandwidth Enhancement Technique on the Noise Performance of CMOS Optical Amplifiers

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Abstract

In this paper, the impact of the inductive peaking bandwidth enhancement technique on the input-referred noise performance of a 10 Gbps optical receiver, which includes the CMOS Regulated Cascode (RGC) Transimpedance Amplifier (TIA) is investigated and analyzed. By examining the noise equations in this paper, a novel low-noise design methodology, is introduced. Additionally, through the implementation of the structured g_m/I_D approach and by selecting the suitable transistor dimensions, the power consumption as well as the noise values are reduced, while the values of the obtained gain and bandwidth are increased. To verify the performance of the designed TIA, the circuit is simulated in HSPICE using 90 nm CMOS technology parameters. The simulation results show the obtained gain value of 55.45 dB Ω , a bandwidth of 7.51 GHz and an input referenced noise value of 15.7 pA/ $\sqrt{\text{Hz}}$ at the 1.2 V power supply, while the circuit consumes 0.75 mW of power.

Keywords g_m/I_D methodology · RGC · Low-power · Low-noise · Transimpedance amplifier (TIA) · Inductive peaking technique · CMOS

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1 Introduction

In the recent years, with new advances in the design of analog integrated circuits for optical communications systems, different performance parameters such as: noise, bandwidth, power consumption and gain can be considered as the major performance measures in design of an optical transimpedance amplifier (TIA) circuit, that is the most important building block in the structure of an optical receiver system. One of the most critical challenges that the circuit designers of such amplifiers always face, is maintaining the proper trade-off between these performance parameters. Therefore, different structures have been reported in the literature to reduce not only the power consumption, but also the noise value of these circuits. In [14], in order to reduce the noise value, noise and signal are passed through two different paths, so that, the signal signs in two different paths are opposite and the noise signs are the same. When these two paths are applied to a differential pair, the noise is removed due to the common mode rejection of the noise in differential structure, which allows the signal amplification by the circuit. However, the main challenge with the technique discussed in [14] is that, employing two amplifiers in two paths and applying the differential signals to the differential structure, demands the higher power consumption while it also increases the chip size area. In [9, 23], a fully-differential structure is employed to remove the common mode noise. By applying the signal to a differential pair amplifier, the noise of the main amplifier and the replica circuit can be effectively eliminated. In [18], a passive inductor is utilized to reduce the noise, while the passive inductor also isolates the large input capacitor at high frequencies in order to reduce the noise value of the circuit.

It is worth mentioning that, employing an inductor in the circuit increases the chip size area. In [1, 8, 10], an alternative method to reduce the noise is reported which involves replacing the main amplifier transistor with a transistor benefiting from the dynamic threshold voltage.

Additionally, the approach reported in [3, 15, 22] explores a noise cancelation technique by using a combination of two paths common gate and a common source structures. This approach generates an opposite phase in the noise signal which effectively cooperates to eliminate the total noise of the circuit.

In [17], the technique of employing several photodiodes to reduce the noise of the circuit is discussed, which requires several amplifiers while it also demands a high power consumption. On the other hand, the g_m/I_D design methodology is employed in [6] and [2, 11, 21] to minimize the power consumption and reduce the noise value, respectively.

In this paper, the impact of adding the bandwidth enhancement inductive peaking technique of a RGC Transimpedance amplifier on the input-referred noise of the circuit, is investigated and analyzed. To properly analyze the impact of employing an active inductor in the RGC circuit on the noise performance, the input-referred noise equations for both the conventional RGC structure and the modified RGC circuit employing the active inductor technique are derived and analytically compared. The noise performances of the modified RGC circuit and conventional RGC TIA are obtained from simulations and compared, which justify that adding an active inductor

structure to a conventional RGC circuit for the same power consumption and gain values, can increase the -3 dB bandwidth of the modified RGC circuit, effectively.

However, considering the trade-off between the power consumption, gain, and bandwidth implies that, the increase in bandwidth leads to the higher noise values of the circuit.

In addition, the simulation results demonstrate that, under the conditions in which the power consumption and gain of the modified RGC circuit remain identical to those of the conventional circuit, an increase in the bandwidth results in elevated noise levels. Therefore, by analyzing the noise equations governing both the conventional RGC and the modified RGC TIA circuit structures, the proposed design methodology introduces a new method to mitigate the noise for a specific power consumption budget.

By implementing the proposed low-power and low-noise design methodology and conducting precise calculations, the dimensions of the major transistors which cooperate effectively in the circuit's noise performance can be properly selected. This ensures that, the noise level in the modified RGC using an active inductor load is reduced to the values below than the conventional RGC circuit. Subsequently, with the application of the structured g_m/I_D design methodology, the power consumption and noise performances are minimized, while the gain and bandwidth performances are optimized through the proper selection of the transistor dimensions.

This paper is organized as follows, in Sect. 2, the structures of the conventional RGC and the modified RGC transimpedance amplifier (which benefits from an active inductor load “inductive peaking technique” to enhance its frequency bandwidth) are introduced and analyzed. In Sect. 3, the noise analysis of both TIA circuits is discussed. In addition, in Sects. 4 and 5, the g_m/I_D design methodology, and the circuit design approach based on g_m/I_D methodology are discussed. The simulation results are presented in Sect. 6, where they are compared with the performances of other reported designs. Finally, some concluding remarks are presented in Sect. 7.

2 Conventional RGC and Modified RGC Structures

Figure 1, shows the basic structure of a conventional RGC circuit [13]. The primary focus of this paper is to investigate the effects of the employment of inductive peaking technique (as a well-known frequency bandwidth extension approach), on the input-referred noise value of a RGC circuit.

To accomplish this, the resistor R_2 in the conventional circuit is replaced by an active inductor load, formed by the combination of two transistors M_4 and M_5 .

Figure 2, illustrates the modified RGC circuit. The impedance seen from the drain of M_4 , denoted as Z_{d1} , and the equivalent realized active inductor represented by L_1 , can be obtained from the Eqs. (1) and (2), respectively [16].

$$Z_{d1} = \frac{r_{o5} \cdot C_{gs4} \cdot S + 1}{g_{m4} + C_{gs4} \cdot S} \quad (1)$$

$$L_1 = \frac{C_{gs4}}{g_{m4}} \left(r_{o5} - \frac{1}{g_{m4}} \right) \quad (2)$$

Fig. 1 Conventional RGC TIA circuit [13]

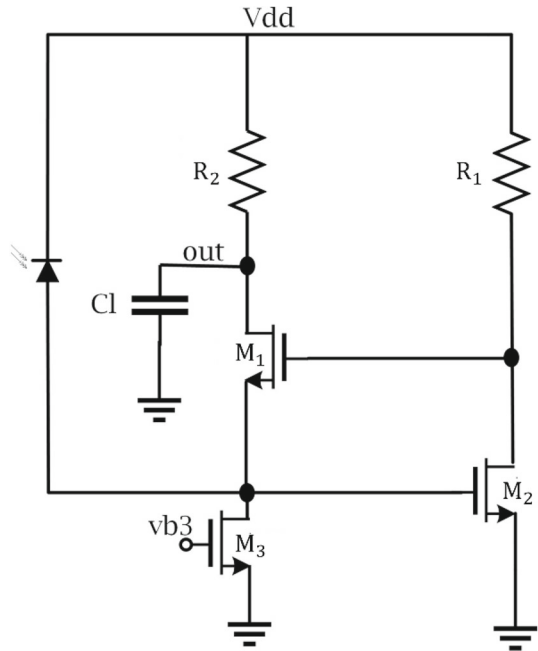
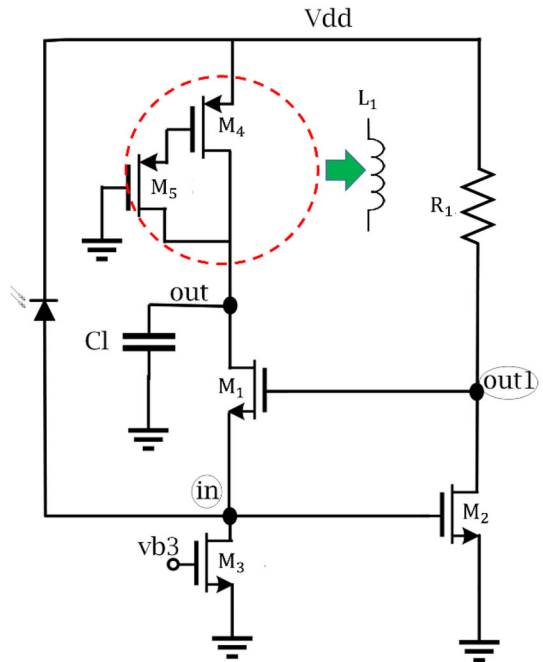


Fig. 2 Modified RGC TIA circuit using active inductor



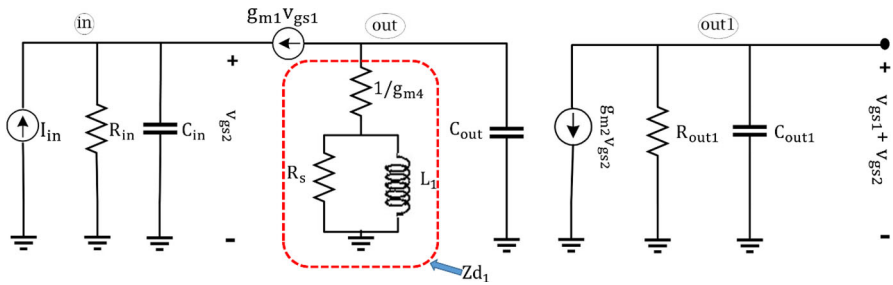


Fig. 3 Small-signal equivalent circuit model for modified RGC circuit

The implemented active inductor, resonates with the capacitor which is seen at the input node, determining the dominant pole, and subsequently shifting it to the higher frequencies. This peaking (resonance) effect enhances the effective frequency bandwidth. On the other hand, employing an active inductor instead of a passive one, results in a smaller chip size area.

Figure 3, shows the small-signal equivalent circuit model of the modified RGC circuit.

The capacitors C_{in} , C_{out} , C_{out1} , and the resistors R_{in} , R_{out} , and R_{out1} , are associated with the nodes of “in”, “out”, and “out1”, respectively [16].

$$C_{in} = C_{PD} + C_{gs2} + \left(1 - \frac{V_{out1}}{V_{in}}\right)(C_{gd2} + C_{gs1}) + C_{gd3} + C_{db3} \quad (3)$$

$$C_{out} = C_1 + \left(1 - \frac{V_{out1}}{V_{out}}\right)C_{gd1} + C_{db1} + C_{db4} + C_{gd5} + C_{db5} \quad (4)$$

$$C_{out1} = C_{db2} + \left(1 - \frac{V_{in}}{V_{out1}}\right)(C_{gd2} + C_{gs1}) + \left(1 - \frac{V_{out}}{V_{out1}}\right)C_{gd1} \quad (5)$$

$$R_{in} = \frac{1}{1 + (1 + A_v)g_{m1}} || r_{o3} \approx \frac{1}{1 + (1 + A_v)g_{m1}} \quad (6)$$

$$A_v = g_{m2}R_{out1} \quad (7)$$

$$R_{out} = (r_{o3}(1 + r_{o1}(g_{m1} + g_{s1})) || Z_{d1} \approx Z_{d1} \quad (8)$$

$$R_s = r_{o5} - \frac{1}{g_{m4}} \quad (9)$$

$$R_{out1} = r_{o2} || R_1 \quad (10)$$

The gain of the modified RGC circuit is obtained as follows:

$$Z_T(S) = \frac{V_{out}}{I_{in}} = \frac{g_{m1}R_{in}(g_{m2}R_{out1} + 1 + R_{out1} \cdot C_{out1} \cdot S)(r_{o5} \cdot C_{gs4} \cdot S + 1)}{(1 + R_{out} \cdot C_{out} \cdot S)(g_{m1}R_{in}(g_{m2}R_{out1} + 1 + R_{out1} \cdot C_{out1} \cdot S) + (1 + R_{out1} \cdot C_{out1} \cdot S)(1 + R_{in}C_{in} \cdot S))(g_{m4} + C_{gs4} \cdot S)} \quad (11)$$

$$Z_T(0) = \frac{g_{m1}R_{in}(g_{m2}R_{out1} + 1)}{(g_{m1}R_{in}(g_{m2}R_{out1} + 1) + 1)g_{m4}} \approx \frac{1}{g_{m4}} \quad (12)$$

In Eq. (13), the input pole is determined as the dominant pole, and the -3 dB cut-off frequency can be derived from Eq. (14) and [16].

$$s_{in} = \frac{1}{C_{in}R_{in}} \quad (13)$$

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_{in}R_{in}} = \frac{1 + (1 + g_{m2}R_{out1})g_{m1}}{(2\pi C_{in})} \quad (14)$$

It is worth mentioning that, one of the advantages of the RGC structure is the utilization of active feedback to decrease the input impedance, while concurrently enhancing the frequency bandwidth according to Eq. (6).

Figure 4, shows the frequency responses of both the conventional RGC TIA and the modified RGC circuits. These simulation results are obtained using identical values for resistor R_1 and the transistors dimensions of M_1 , M_2 , and M_3 , in both circuits, ensuring the power consumption values are consistent. The dimension of transistor M_4 is adjusted to ensure obtaining equal gain values for both circuits. To properly implement an inductive peaking effect, the zero frequency location is strategically placed near the dominant pole frequency. This is achieved by modifying the dimensions of transistor M_5 to create a maximum peak of 0.7 dB while enhancing the effective frequency bandwidth without an undesired increase in the power consumption value.

As depicted in Fig. 4, the frequency bandwidth significantly increases from 4.44 to 8.81 GHz. Figure 5, illustrates the average input-referred noise value obtained at 7 GHz bandwidth. The increased noise value of the modified RGC circuit indicates that, adding the active inductor technique to the conventional RGC circuit, has led to an increase in the noise value of the circuit. This observation affirms that, while the

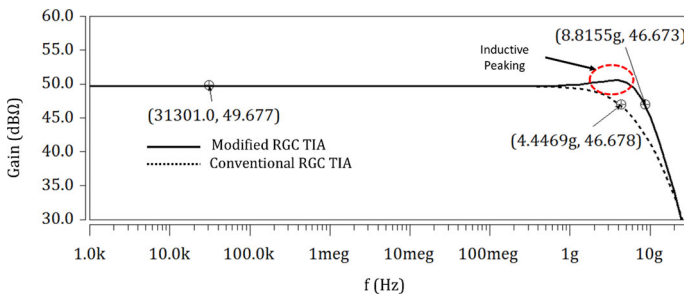


Fig. 4 Frequency responses of the conventional RGC TIA and the modified RGC circuits

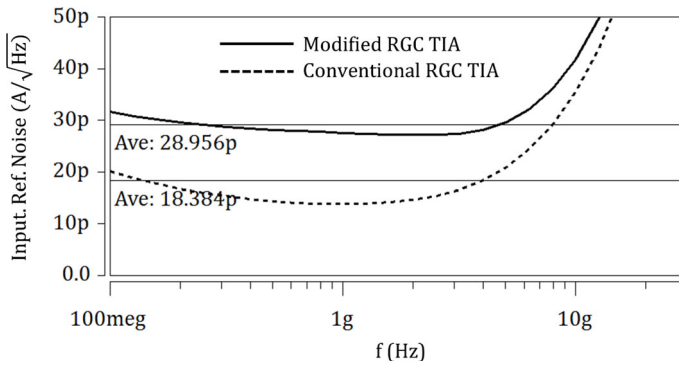


Fig. 5 Input-referred noise comparison at 7 GHz bandwidth, for both the conventional RGC TIA and the modified RGC circuits

active inductor enhances bandwidth, this frequency bandwidth enhancement comes at the cost of increased input-referred noise for the TIA circuit structure.

Consequently, this paper focuses on devising a new solution to mitigate the additional noise introduced by the inductive peaking bandwidth extension technique. This involves an examination of the noise-governing equations and also g_m/I_D transistor sizing approach.

3 Noise Analysis

In Fig. 6, the thermal noise sources of the modified RGC circuit are presented. Due to the fact that, transistor M_1 forms a common gate (CG) stage, the noise current generated by this transistor can be disregarded [16]. The total input-referred noise is the aggregate of the input-referred noise values obtained for transistors M_2 , M_3 , M_4 , M_5 and the resistor R_1 , which is expressed in Equation (20).

$$\overline{I_{n.in}^2} = \overline{I_{n.M_2}^2} + \overline{I_{n.R_1}^2} + \overline{I_{n.M_4}^2} + \overline{I_{n.M_5}^2} \quad (15)$$

$$\overline{I_{n.M_2}^2} + \overline{I_{n.R_1}^2} = 4KT\gamma \left(\frac{1}{g_{m2}} + \frac{1}{\gamma R_1 \cdot g_{m2}^2} \right) \left(C_{in}^2 s^2 + \frac{1}{R_{in}^2} \right) \quad (16)$$

$$\overline{I_{n.M_3}^2} = 4KT\gamma(g_{m3}) \quad (17)$$

$$\overline{I_{n.M_4}^2} = 4KT\gamma(g_{m4}) \quad (18)$$

$$\overline{I_{n.M_5}^2} = 4KT\gamma(g_{ds.M_5}) \quad (19)$$

$$\overline{I_{n.in}^2} = 4KT\gamma \left[(g_{m3} + g_{m4} + g_{ds.M_5}) + \left(\frac{1}{g_{m2}} + \frac{1}{\gamma R_1 \cdot g_{m2}^2} \right) \left(C_{in}^2 s^2 + \frac{1}{R_{in}^2} \right) \right] \quad (20)$$

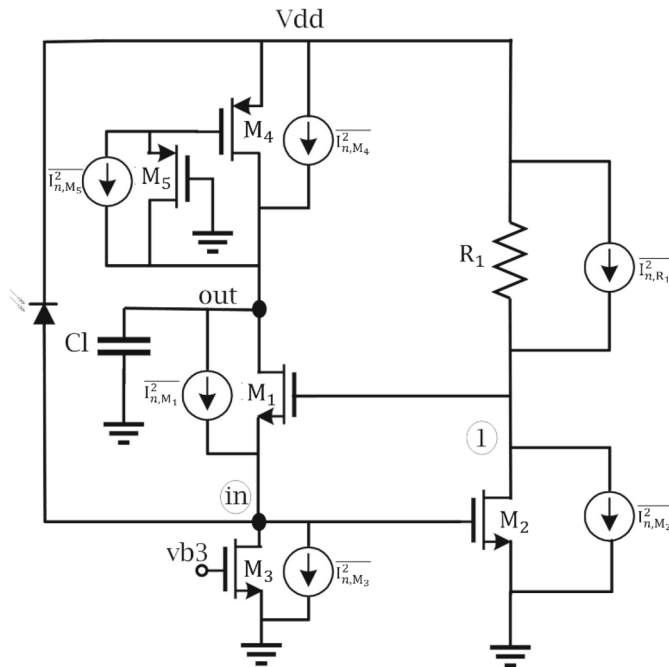


Fig. 6 Equivalent noise circuit model of the modified RGC circuit

where, k represents the Boltzmann constant and γ is the thermal noise coefficient of the transistor channel. The input-referred noise in the conventional RGC TIA circuit can be determined using the following equation:

$$\overline{I_{n,in}^2} = 4KT\gamma \left[\left(g_{m3} + \frac{1}{\gamma R_2} \right) + \left(\frac{1}{g_{m2}} + \frac{1}{\gamma R_1 \cdot g_{m2}^2} \right) \left(C_{in}^2 s^2 + \frac{1}{R_{in}^2} \right) \right] \quad (21)$$

When comparing the two equations (Eqs. (20) and (21)), for the input-referred noise in modified RGC TIA and the conventional RGC circuits, it is obvious that, the second term of both equations is identical. The distinction is in the first term of Eq. (21), the term $\frac{1}{\gamma R_2}$ is replaced by $g_{m4} + g_{ds,M5}$ which is from Eq. (20).

Therefore, deducing from the noise diagram in Fig. 5, the increase in the noise value in the modified RGC circuit, is primarily attributed to this term difference and the noise of the transistors M_4 and M_5 is directly added to the input node. Hence, the underlying principle of the low-noise design methodology in the modified RGC circuit is:

If the dimensions of the transistors are designed such that, the term: $g_{m4} + g_{ds,M5} < \frac{1}{\gamma R_2}$, then, the noise value in the modified RGC circuit is expected to be lower than the noise value of the conventional RGC TIA circuit. To achieve $g_{m4} + g_{ds,M5} < \frac{1}{\gamma R_2}$, it is necessary to reduce the values of g_{m4} , $g_{ds,M5}$.

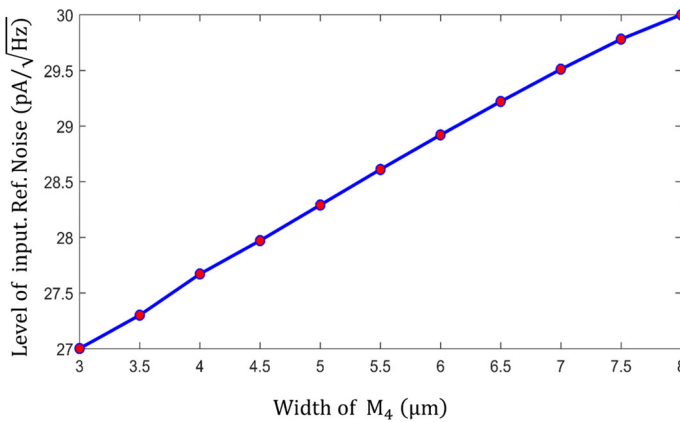


Fig. 7 The effect of reducing the width of transistor M_4 on the value of input-referred noise

Initially, decreasing the transistor width of W_4 , as shown in Fig. 7, slightly decreases the noise value from 30 to 27 $\text{pA}/\sqrt{\text{Hz}}$. However, this reduction in W_4 , also decreases the voltages at nodes “in” and “out”, resulting in a lower g_{m2} value. This decrease in g_{m2} may cause transistor M_2 to enter in the cut-off region, which leads to an increase in the input-referred noise value, as it is expressed in Eq. (20).

In addition, to decrease the $g_{ds,M5}$ value, reducing W_5 is an option. However, changing W_5 affects the zero frequency, removing the peaking effect that is seen in the frequency response, and significantly limits the total frequency bandwidth. This limitation is undesirable in the proposed design and thus reducing W_5 does not have noticeably impact on the reduction of the overall noise value in the circuit.

Furthermore, transistor M_4 acts as an active load and transistor M_5 acts as a resistor and the current flowing through the M_5 is approximately negligible. If the drain current I_{D4} decreases, the transconductance of M_4 (g_{m4}) also decreases, resulting in a reduction in the noise value as it can be seen in Eq. (20). Additionally, in the modified RGC circuit depicted in Fig. 2, transistor M_3 operates as a current source, and I_{D3} , equals I_{D4} . Thus, decreasing the width of the M_3 , concurrently reduces the currents of the M_3 and the M_4 transistors. This reduction in W_3 affects some factors in the noise performance, as expressed in Eq. (20), leading to a simultaneous decrease in g_{m3} and g_{m4} parameters.

However, according to Eq. (20), both the g_{m3} and g_{m4} parameters directly influence the circuit's noise performance. On the other hand, a decrease in W_3 results in an increase in the drain-source voltage of the transistor M_3 (V_{DS3}). The value of V_{DS3} is equivalent to the gate-source voltage of the transistor M_2 , and an increase in V_{GS2} raises the value of g_{m2} parameter, as it can be seen in Eq. (20). This increase in g_{m2} contributes to a reduction in the noise value. Therefore, reducing the width of W_3 can be considered as the optimal solution to satisfy the equation condition of:

$$g_{m4} + g_{ds,M5} < \frac{1}{\gamma R_2}.$$

The graph in Fig. 8, illustrates the impact of reducing the width of transistor M_3 on the noise reduction. The intersection of $g_{m4} + g_{ds,M5}$ and $\frac{1}{\gamma R_2}$ diagrams are shown in

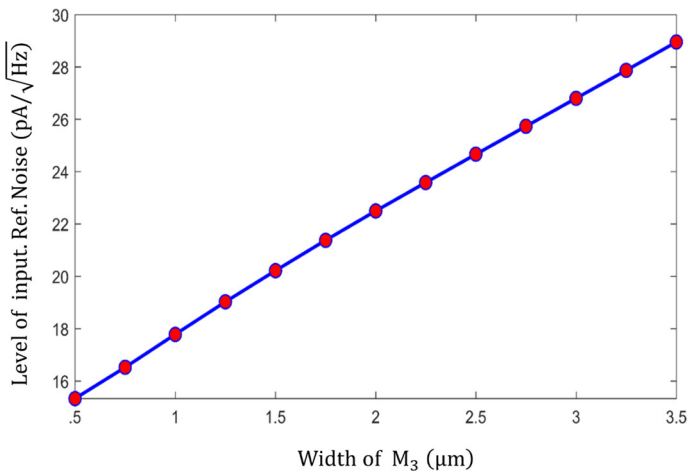


Fig. 8 The effect of reducing the width of transistor M_3 on the value of input-referred noise

Fig. 9. Moreover, Table 1, summarizes the effect of varying the width of W_3 , on the drain current of M_3 , gain, bandwidth, noise, and $g_{m4} + g_{ds,M_5}$ (mU) parameters.

The results obtained from Table 1, and the graph shown in Fig. 8, support the assertion that, decreasing W_3 and subsequently the reduction of I_{D3} , leads to a reduction in the noise value of the circuit. Figure 9 indicates that, for $W_3 < 1.4 \mu\text{m}$, the equation $g_{m4} + g_{ds,M_5} < \frac{1}{\gamma R_2}$ can be realized. Moreover, according to Table 1, for $W_3 < 1 \mu\text{m}$, the noise in the modified RGC circuit is less than $17.78 \text{ pA}/\sqrt{\text{Hz}}$, surpassing the conventional RGC TIA circuit's noise at $18.38 \text{ pA}/\sqrt{\text{Hz}}$.

Thus, selecting W_3 value below $1 \mu\text{m}$, allows simultaneous reduction in noise, power consumption, and an increase in the gain performance to be occurred. Although, a slight decrease in the effective frequency bandwidth may occur, it aligns with the expectations of benefiting from these advantages.

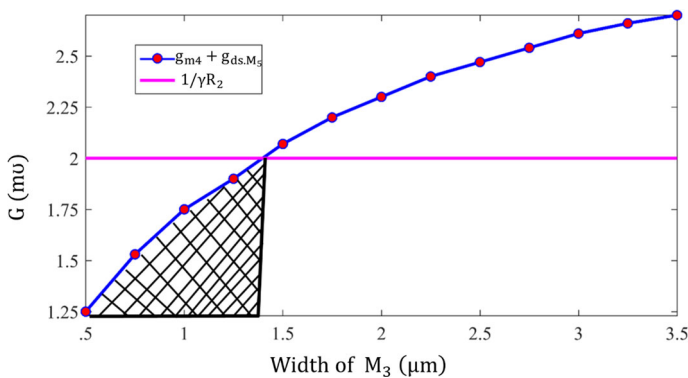


Fig. 9 The intersection of $g_{m4} + g_{ds,M_5}$ and $\frac{1}{\gamma R_2}$ parameter diagrams

Table 1 Effect of width variation for M_3 on the values of: input-referred noise, I_{D3} , Gain, Bandwidth and $g_{m4} + g_{ds,M_5}$ parameters

$W_3(\mu m)$	0.5	0.75	1	1.25	1.5	1.75	2	2.25	2.5	2.75	3	3.25	3.5
$I_{D3}(\mu A)$	73	110	145	180	215	250	284	318	352	385	417	450	482
Input.Ref.Noise (pA/ $\sqrt{Hz}$)	15.33	16.52	17.78	19.02	20.21	21.37	22.49	23.58	24.66	25.73	26.8	27.87	28.95
Gain (dB Ω)	58.53	56.26	54.8	53.75	52.95	52.31	51.78	51.33	50.93	50.57	50.25	49.95	49.67
Bandwidth (GHz)	2.8	4.16	5.4	6.51	7.28	7.81	8.19	8.49	8.7	8.86	8.84	8.83	8.81
$g_{m4} + g_{ds,M_5}$ (mS)	1.25	1.53	1.75	1.9	2.07	2.2	2.3	2.4	2.47	2.54	2.61	2.66	2.71

Certainly, for designing the modified RGC circuit, the g_m/I_D design methodology can be effectively employed alongside with the low-noise design methodology. The combination of these two approaches enables the designer to optimize the performances of power consumption, bandwidth, gain, and noise of the circuit, simultaneously.

4 g_m/I_D Design Methodology

The g_m/I_D design methodology is employed for design of analog circuits and determining optimal transistor dimensions more efficiently. This technique, utilizes a technology-dependent characteristic curve, that remains independent of the transistor dimensions, encompassing all the transistor operation regions such as strong inversion, moderate inversion, and weak inversion. Essentially, it aids in designing proper transistor dimensions within a specified fabrication technology, taking into account each transistor’s role in the circuit and its appropriate operation region. Table 2, provides a summary of the main characteristics of the transistor operation regions.

The transistor’s operation is selected based on its circuit role as a current source, amplifier, or active inductor in the circuit, respectively. This methodology replaces the design variables from transistor dimensions (W , L) to normalized drain current value $I_n = I_D/(W/L)$ and the (g_m/I_D) parameter which is derived from the g_m/I_D characteristic curve, for each transistor. By using the g_m/I_D parameter and I_D values corresponding to the pre-determined roles of the transistors from Table 3, the transistor dimensions (W , L) can be easily resulted through the g_m/I_D characteristic curve. Figure 10, depicts the g_m/I_D characteristic curve in terms of normalized drain current $I_n = I_D/(W/L)$, for all the NMOS and PMOS transistors in 90 nm technology.

By determining the values of (g_m/I_D) parameter and I_n , the dimensions of each transistor can be obtained through the utilization of the g_m/I_D characteristic curve.

Based on the aforementioned details, the design methodology including the transistor sizing algorithm for the modified RGC circuit is illustrated in Fig. 11.

Table 4, summarizes the dimensions obtained from applying the g_m/I_D design methodology to the modified RGC utilizing the proposed low-noise design approach.

Table 2 Main characteristic of each bias region

Inversion region	Characteristic of region
Weak inversion	Low-power, high-gain
Moderate inversion	Moderate gain and bandwidth
Strong inversion	High-speed (bandwidth), high-power consumption

Table 3 Simulated performance parameters for the proposed design

Performance parameter	Required value	HSPICE (Simulated)
DC gain (dBΩ)	≥ 53	55.45
BW (GHz)	≥ 6.5	7.51
Power consumption (mW)	Minimize	0.75
Noise ($\frac{\text{pA}}{\sqrt{\text{Hz}}}$)	< 18	15.7
$\left(\frac{g_m}{I_D}\right)_1$	[9–19]	14.18
$\left(\frac{g_m}{I_D}\right)_2$	[9–19]	12.23
$\left(\frac{g_m}{I_D}\right)_3$	[3–9]	7.3
$\left(\frac{g_m}{I_D}\right)_4$	[9–19]	11.25
$\left(\frac{g_m}{I_D}\right)_5$	[3–9]	4.64

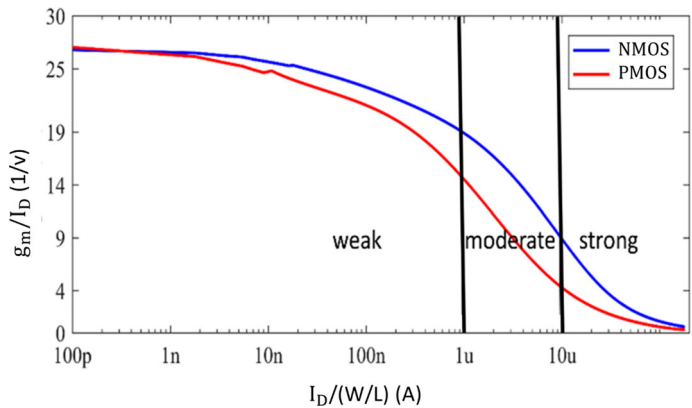


Fig. 10 Simulated (g_m/I_D) characteristic curve obtained in 90 nm CMOS technology

5 The Circuit Design Based on the g_m/I_D Methodology

To formulate the design of the modified RGC circuit based on the g_m/I_D methodology, Eqs. (12), (14), and (20) expressing gain, -3 dB cutoff frequency, and noise can be re-written in terms of the two new design variables of (g_m/I_D) and I_D :

$$A_v(s = 0) \approx \frac{1}{g_{m4}} = \frac{1}{I_{D4}\left(\frac{g_m}{I_D}\right)_4} \tag{22}$$

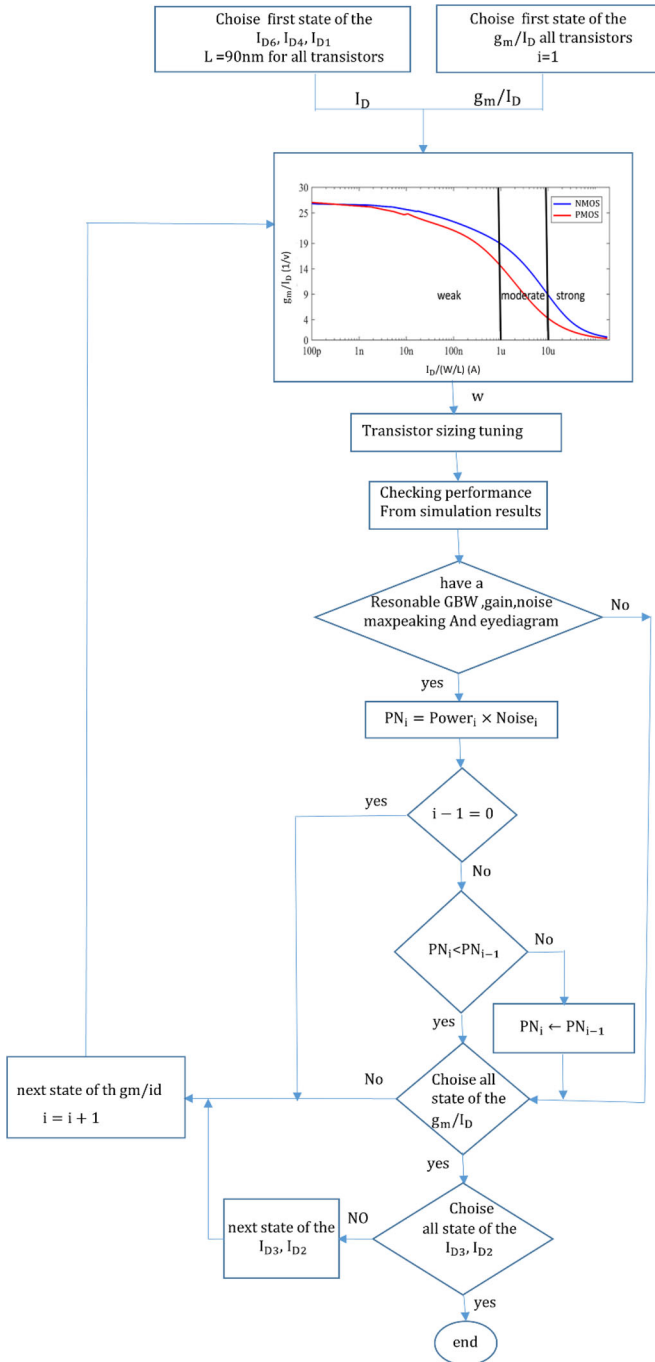


Fig. 11 Proposed design methodology

Table 4 TIA transistor dimensions

Component	Parameter value
M ₁	W/L = 3.3 $\mu\text{m}/0.09 \mu\text{m}$
M ₂	W/L = 8 $\mu\text{m}/0.09 \mu\text{m}$
M ₃	W/L = 0.9 $\mu\text{m}/0.09 \mu\text{m}$
M ₄	W/L = 6 $\mu\text{m}/0.09 \mu\text{m}$
M ₅	W/L = 0.5 $\mu\text{m}/0.09 \mu\text{m}$
R1	700 Ω

$$f_{-3\text{dB}} = \frac{1 + (1 + g_{m2}R_{\text{out}1})g_{m1}}{(2\pi C_{\text{in}})} = \frac{1 + \left(1 + \frac{\left(\frac{g_m}{I_D}\right)_2 R_2}{1 + R_2 \tau_2}\right) I_{D1} \left(\frac{g_m}{I_D}\right)_1}{(2\pi C_{\text{in}})} \quad (23)$$

$$\begin{aligned} \overline{I_{n,\text{in}}}^2 &= 4KT\gamma \left[(g_{m3} + g_{m4} + g_{\text{ds},M_5}) + \left(\frac{1}{g_{m2}} + \frac{1}{\gamma R_1 \cdot g_{m2}^2} \right) \left(C_{\text{in}}^2 s^2 + \frac{1}{R_{\text{in}}^2} \right) \right] \\ &= 4KT\gamma \left[I_{D3} \left(\left(\frac{g_m}{I_D} \right)_3 + \left(\frac{g_m}{I_D} \right)_4 \right) \right. \\ &\quad \left. + \gamma I_{D5} + \left(\frac{1}{I_{D2}} \frac{1}{\left(\frac{g_m}{I_D} \right)_2} + \frac{1}{I_{D2}^2} \frac{1}{\gamma R_1 \left(\frac{g_m}{I_D} \right)_2^2} \right) \left(C_{\text{in}}^2 s^2 + \left[1 + \left(1 + \frac{\left(\frac{g_m}{I_D} \right)_2 R_2}{1 + R_2 \tau_2} \right) I_{D1} \left(\frac{g_m}{I_D} \right)_1 \right]^2 \right) \right] \quad (24) \end{aligned}$$

6 Simulation Results

This section presents the simulation results for the proposed design methodology. Figures 12 and 13, show the impact of employing both the low-noise design methodology and the g_m/I_D methodology, on the frequency response and noise performances of the modified RGC circuit. These results are also compared with those obtained for the conventional RGC TIA circuit.

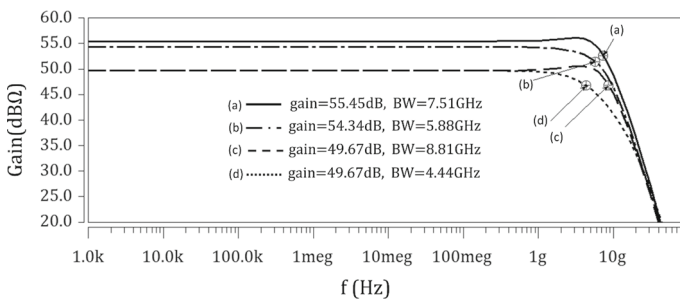


Fig. 12 Frequency responses of the (a) modified RGC using the proposed low-noise design methodology and g_m/I_D technique, (b) modified RGC using the proposed low-noise design methodology, (c) Modified RGC without low-noise design methodology and g_m/I_D technique, (d) Conventional RGC TIA

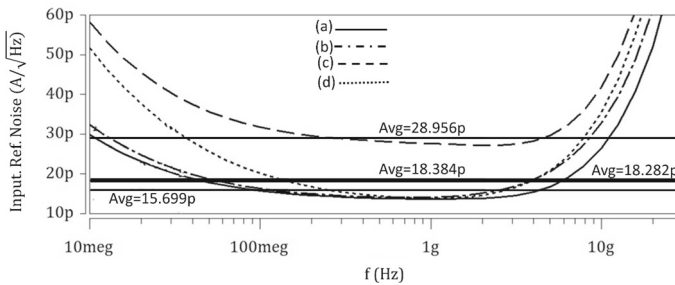


Fig. 13 Input-referred noise obtained at 7 GHz bandwidth of the (a) modified RGC using the proposed low-noise design methodology and g_m/I_D technique, (b) Modified RGC using the proposed low-noise design methodology technique, (c) modified RGC without low-noise design methodology and g_m/I_D technique, (d) Conventional RGC TIA

In Fig. 12, the frequency response of the modified RGC is depicted, utilizing the proposed low-noise design methodology and g_m/I_D technique. As it is discussed in Sect. 2, the active inductor L_1 is formed by two transistors M_4 and M_5 . By adjusting the channel width of the M_5 , the zero frequency location caused by this active inductor can be shifted to proper frequencies. This adjustment is made to ensure that, the dominant pole becomes less influential, resulting in an increased bandwidth without an increase in the power consumption. Notably, a gain of 55.45 dB Ω and bandwidth of 7.51 GHz are achieved for a power consumption of 750 μ W at a 1.2 V supply.

In Fig. 13, the average input-referred noise performance of the modified RGC is displayed, utilizing the proposed low-noise design methodology and g_m/I_D technique at a 7 GHz frequency bandwidth. By comparing with the graph presented in Fig. 5, it is revealed that, the combination employment of low-noise design approach and the g_m/I_D design methodology, is highly effective in reducing the overall noise of the system. In other words, the noise value decreases from 28.95 to 15.7 pA/ $\sqrt{\text{Hz}}$, representing a significant (45.7%) reduction in the noise value, thanks to the use of the proposed design methodology.

To evaluate the output signal quality of the modified RGC using the proposed low-noise design methodology and g_m/I_D technique, the circuit is simulated for two different input signals with amplitudes of 50 μ App, 100 μ App, at a bit rate of 10Gbps NRZ PRBS¹ ($2^7 - 1$). Figure 14, shows the output signal eye diagrams obtained for these two input current levels. It is evident that, the vertical eye range is sufficiently open, indicating the proper output swing for the proposed design.

The vertical eye opening ranges are equal to 27.1 mVpp for a 50 μ App input current signal and 55 mVpp for a 100 μ App input current signal.

To analyze the non-ideal effects arising from the non-ideal fabrication process, and investigate the impact of the undesired variations in transistor dimensions on the circuit's overall performance, the MONTE-CARLO analysis is performed for 500 different runs. This involves applying a 10% change in the transistors dimensions. The simulation results obtained for the gain and bandwidth performances of the designed TIA, are presented in Fig. 15a.

¹ Non-Return-to-Zero Pseudo Random Binary Sequence.

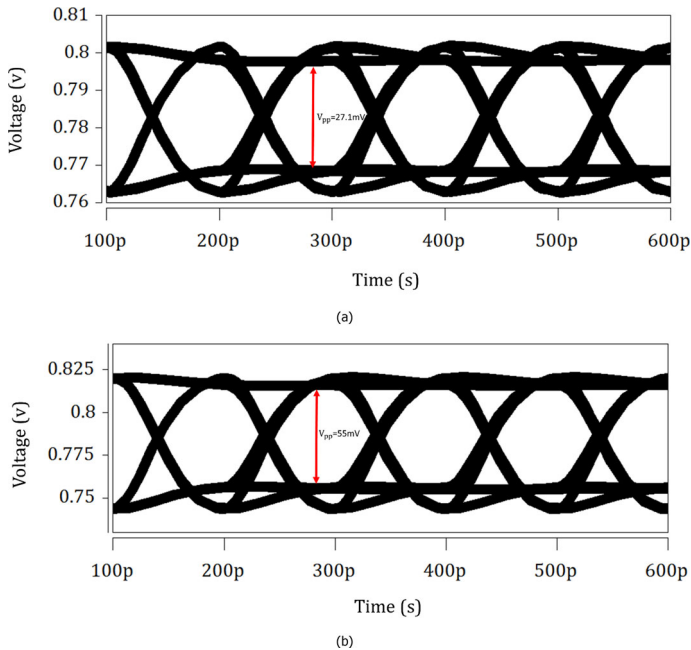


Fig. 14 Simulated eye-diagram using 10 Gb/S PRBS (2^7-1) of the modified RGC using the proposed low-noise design methodology and g_m/I_D technique for input current of **a** 50 μ App, **b** 100 μ App

According to Fig. 15b, the mean-value of the gain performance parameter for the TIA is obtained as of 55.4 dB Ω , with a standard deviation of 0.40 dB Ω .

In Fig. 15c, the average bandwidth of the circuit is obtained as of 7.56 GHz, with a standard deviation of 0.34 GHz.

To evaluate the temperature performance of the modified RGC circuit utilizing the proposed low-noise design methodology and g_m/I_D technique, the impact of changing the temperature on the values of the key performance parameters such as gain and – 3 dB cut-off frequency, is investigated. The obtained temperature simulation results are presented in Fig. 16 and summarized in Table 5.

In addition, considering the simulation results summarized in Table 6, it is evident that, adding the active inductor structure to the conventional RGC circuit has led to a notable increase in the noise value. This can be mitigated by making proper adjustments to the dimensions of M_3 , that acts as a current source, and M_5 transistor, which serves as a resistance in the RGC with active inductor circuit.

Furthermore, it is worth mentioning that, the noise of the circuit has been reduced from 28.95 to 15.7 pA/ $\sqrt{\text{Hz}}$, resulting in a 45.7% reduction, due to the implementation of the low-noise design methodology. In addition, the power consumption is reduced from 0.81 to 0.75 mW, while the gain has increased from 49.67 to 55.45 dB Ω .

In Table 7, simulation results of the modified RGC circuit using the proposed low-noise design methodology and g_m/I_D technique are compared with performances reported from previously published TIA structures. Notably, the power consumption

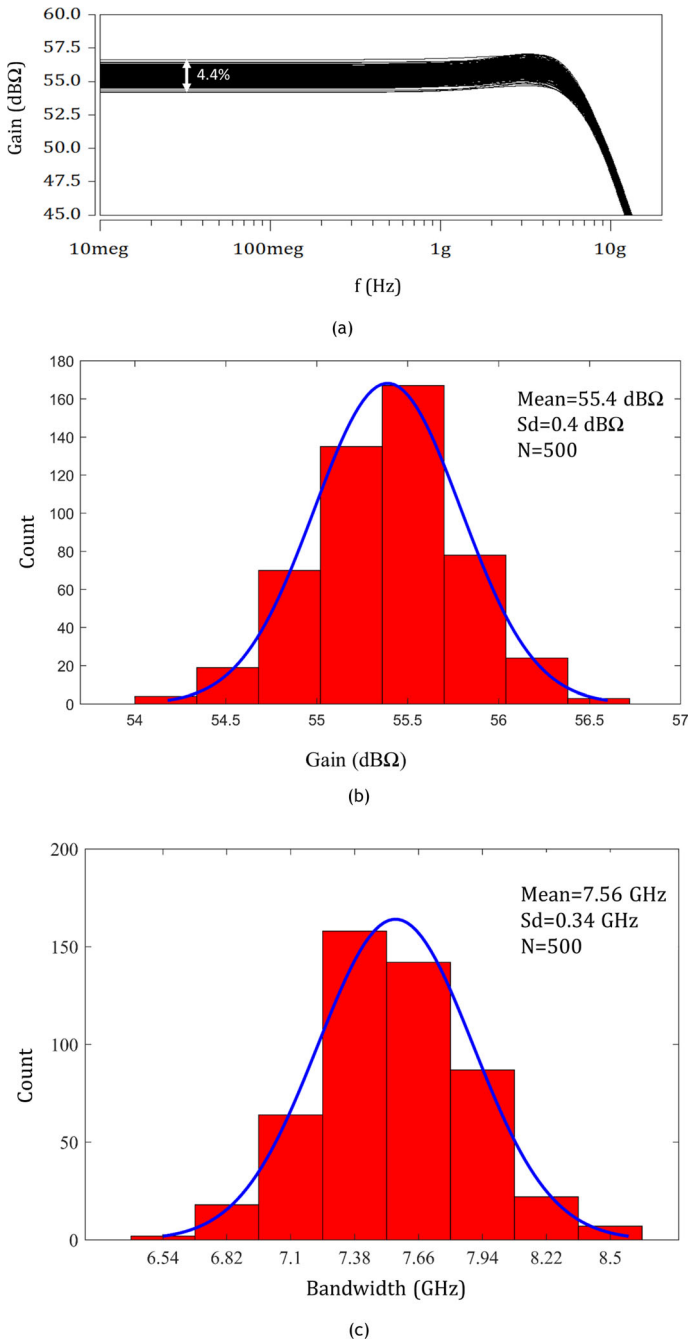


Fig. 15 Monte-Carlo analysis with 10% mismatch **a** frequency response, **b** gain **c** bandwidth of the modified RGC using the proposed low-noise design methodology and g_m/I_D technique circuit

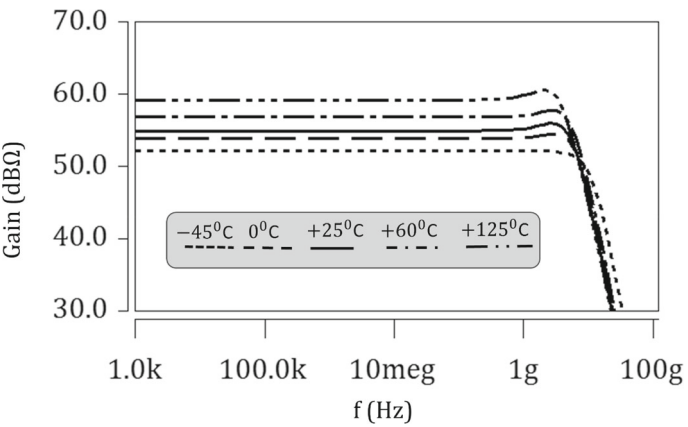


Fig. 16 Effect of temperature variations on the frequency response performance of the modified RGC using the proposed low-noise design methodology and g_m/I_D technique circuit

Table 5 Effect of temperature variations on the values of frequency bandwidth, and TIA gain

	– 45°C	– 25°C	0°C	+ 55°C	+ 60°C	+ 80°C	+ 125C
Gain (dBΩ)	52.18	53.1	54.28	55.37	56.79	57.56	59.2
Bandwidth (GHz)	9.7	9.3	8.5	7.5	6.4	5.80	4.7
Power consumption (mW)	0.77	0.77	0.76	0.75	0.73	0.73	0.71
Noise ($\frac{pA}{\sqrt{Hz}}$)	15.39	15.52	15.63	15.69	15.76	15.83	16.15

Table 6 Performance comparison of conventional RGC TIA, modified RGC, and modified RGC using the proposed low-noise design methodology and g_m/I_D technique topologies considered in the low-noise design methodology

	Gain (dBΩ)	Bandwidth (GHz)	Power (mW)	Noise ($\frac{pA}{\sqrt{Hz}}$)
Conventional RGC TIA	49.67	4.45	0.86	18.38
Modified RGC	49.67	8.81	0.81	28.95
Modified RGC circuit using the proposed low-noise design methodology and g_m/I_D technique	55.45	7.51	0.75	15.7

Bold values show the performance of our technique

Table 7 Performance comparison between the modified RGC circuit using the proposed low-noise design methodology and g_m/I_D technique and other reported designs

Ref	[4]	[18]	[23]	[5]	[14]	[19]	[12]	[20]	[7]	This work
Year	2013	2017	2018	2018	2019	2020	2021	2022	2022	2023
Technology	40 nm CMOS	180 nm CMOS	90 nm CMOS	180 nm CMOS	90 nm CMOS	180 nm CMOS	130 nm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS
Supply voltage(V)	1.1	1.8	1	1.8	1.2	1.8	1.3	1	1	1.2
Power consumption (mW)	2.03	18	1.4	5	3.6	4.3	12.2	23.9	29	0.75
Gain (dBΩ)	47	59	40.5	59.7	60	51.4	47	46	40	55.45
Bandwidth (GHz)	8	7.9	7	7.38	7	7.3	10.1	11.4	25.85	7.51
Input-referred noise ($\frac{pA}{\sqrt{Hz}}$)	22	23	20.3	12.2	9.5	27	42	46.6	25	15.7
CPD (fF)	450	300	200	250	325	250	1000	100	–	200
Number of inductors		2	–	–	–	–	–	–	–	–
FOM1	882.2	391	529.63	1425.89	1944.44	630.74	185.33	95.17	89.13	5930.33
FOM2	18.04	5.1	5.22	29.22	66.52	5.84	4.41	0.2	–	75.54
Work	Measured	Simulated	Simulated	Simulated	Simulated	Simulated	Simulated	Measured	Measured	Simulated

of the proposed design is considered as the minimum value in comparison with other reported designs. Furthermore, the noise performance of the proposed design is superior to all the previous designs, except those reported in [5] and [14]. However, it is worth mentioning that, the lower noise values reported in designs [5] and [14], are achieved at the cost of higher power consumption values compared to the proposed design in this paper.

Therefore, as it is obvious in Table 7, the design reported in [7], achieves the maximum frequency bandwidth. But, this high bandwidth is achieved at the cost of a minimum gain value and the highest power consumption value among the different compared designs. Additionally, its noise performance is as favorable as the proposed design.

To ensure a fair performance comparison for the modified RGC circuit structure using the proposed low-noise design methodology and g_m/I_D technique with other reported TIA designs, two different Figures of Merit, (FOM1) and (FOM2), based on the Eqs. (25) and (26) [23], are employed. These FOM parameters consider all the effective design performance parameters including: power consumption, bandwidth, input-referred noise and the value of the input capacitor of the circuit. As it can be seen in Table 7, the proposed low-power and low-noise design methodology provides superior overall performance in terms of the both figure of merit (FOM) values, justifying the commendable performance of the proposed design compared to other reported designs.

$$\text{FOM1} = \frac{\text{Gain } (\Omega) \times \text{Bandwidth (GHz)}}{\text{Power consumption (mW)}} \quad (25)$$

$$\text{FOM2} = \frac{\text{Gain } (\Omega) \times \text{Bandwidth (GHz)} \times C_{in} \text{ (pF)}}{\text{Power consumption (mW)} \times \text{input-referred Noise } \left(\frac{\text{pA}}{\sqrt{\text{Hz}}} \right)} \quad (26)$$

7 Conclusions

In this paper, the impact of adding an active inductor (inductive peaking technique) to enhance the -3 dB effective frequency bandwidth on the input-referred noise performance of the TIA circuit, is investigated and analyzed. The incorporation of an active inductor in a conventional RGC TIA circuit, enhanced the frequency bandwidth from 4.44 to 8.81 GHz, while as a cost to this frequency bandwidth enhancement, it increases the input-referred noise value from 18.38 to 28.95 pA/ $\sqrt{\text{Hz}}$. Therefore, as a solution to this issue, through the simultaneously employment of both the low-noise design methodology and g_m/I_D design technique, the modified RGC circuit achieved a significant (45.7%) reduction in the input-referred noise value (from 28.95 to 15.7 pA/ $\sqrt{\text{Hz}}$), while it achieved the nearly doubled gain value (increased from 49.67 to 55.45 dB Ω), benefits from a reduction in the power consumption value (from 0.81 to 0.75 mW).

Finally, by performing a performance comparison with other reported designs, it is highlighted that, the designed inductive-peaking based RGC TIA circuit which

employs both the low-noise design methodology and the g_m/I_D design approach, provides superior overall performance in terms of noise, power consumption, gain, and frequency bandwidth in comparison with other reported designs.

Data Availability Data sharing does not applicable to this article as no datasets were generated or analyzed during the current study.

Declarations

Conflict of interest There is no Funding and conflicts of interests applicable to this article and this study.

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