

6.2 A 112.5Gb/s ADC-DSP-Based PAM-4 Long-Reach Transceiver with >50dB Channel Loss in 5nm FinFET

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With increasing demand in next-generation data centers and high-performance computing and networking, wireline transceivers are required to operate at 112Gb/s to provide high bandwidth [1-3], meanwhile it is necessary to handle >40dB insertion loss to support legacy channels and large package designs [4]. Low-power design is also critical for the integration of multiple transceivers [5]. To advance state-of-the-art design, this work presents an ADC/DAC-DSP based PAM-4 transceiver capable of equalizing >50dB lossy channels and achieving 112.5Gb/s per channel in a 5nm FinFET process with a power efficiency of 4.5pJ/b.

The SerDes architecture is shown in Fig. 6.2.1, the quad macro consists of a 4-lane PAM-4 112.5Gb/s transceiver and a common block which includes bandgap, current and voltage generator, regulators, and a temperature sensor. The receiver (RX) frontend consists of an input termination network, a 2-stage continuous-time linear equalizer (CTLE) and a 7b 56GS/s 64-way time-interleaved (TI) SAR-ADC. The receiver DSP consists of data path equalizer and a parallel clock recovery path. An LMS engine adapts the equalizer and calibration logic corrects the TI-ADC gain, offset and sampling clock skew. The quarter-rate clocking scheme transmitter (TX) consists of a 56GS/s 7.5b voltage mode DAC driver, 4-to-1 and 40-to-4 serializers, and a 6-tap FIR filter. Each lane has an LC-PLL for independent configuration and providing clocks to RX and TX with a power-supply-regulated CMOS buffer. The LC-VCO has a frequency range of 10-16GHz and can support a seamless data rate range of 1-to-112.5Gb/s with a divide-by-1.5 circuit.

The RX architecture is shown in Fig. 6.2.2. It is optimized to achieve minimal power consumption and efficiently cover a wide data rate range from 1 to 112.5Gb/s for both NRZ and PAM-4 modulations. The input network makes use of inductors to distribute the bump and ESD capacitance, and a separate inductor to resonate out the CTLE input capacitance to extend the input bandwidth. The termination resistance is calibrated to 50Ω and can be configured to accommodate both AC and DC coupled applications. The CTLE provides up to 18dB peak gain and is made of two stages as shown in Fig. 6.2.3. The first stage is a G_m with inductive loading and resistance and capacitance degeneration, it is also used to compensate for gain variation across temperature through an automatic gain control (AGC) loop. The second stage is a trans-admittance trans-impedance (TAS-TIS) topology with inductive feedback and degeneration control. The second stage provides coarse gain control through feedback resistance and its trans-impedance output stage is efficient for driving the large load presented by the T&H circuits. Both CTLE stages have extensive controls that provide tuning for performance at the highest data rate and can be reconfigured to shift peaking frequency to efficiently support lower data rates.

The CTLE drives 8-way interleaving T&H switches as shown in Fig. 6.2.3. The T&H switches are optimized for BW, while minimizing signal feedthrough, asymmetric clock coupling and signal-dependent charge injection. The T&H switches have a 2UI tracking time, and a 6UI hold time. A sampled signal is buffered through a flipped voltage source follower to drive one SAR ADC CDAC at a time; there are a total of 8 SAR ADCs per T&H path. In order to scale power efficiently, the T&H circuit changes from 8-way interleaving to 4, to 2, to 1 track and hold path as data rate is reduced, thus the number of ADCs used at lower data is also reduced. The SAR ADC is a 7b design with non-binary weighting and uses asynchronous operation to maximize efficiency and optimize the metastability error rate. The ADC has a programmable regulated supply for the comparator to optimize speed and power consumption across process corners. The ADC resolution and input dynamic range are also adaptive to further enhance efficiency in meeting design targets. The TI-ADC uses offset and gain start-up and background calibrations that are entirely implemented in the digital signal path. Skew calibration detection which aligns the T&H sampling clock edges to be 1UI apart is implemented in the digital domain, and the skew correction control is fed back to analog T&H skew correction circuits. The ADC SAR slice runs at 875MHz and the whole TI-ADC runs at an 56GS/s. The RX clock comes from the PLL macro. The 8-phase clocks for the phase interpolator (PI) are generated from a DLL after duty cycle correction. The Phase interpolator (PI) is driven by a DSP-based CDR loop and its output clock is used to generate 8-phase 7G clocks with 1UI separation for 8 T/H circuits.

Referring to Fig. 6.2.2, the RX DSP data path is composed of a 22-tap FFE, a 1-tap speculative DFE and an 8-tap floating tap FFE which can be moved up to 120UI for reflection cancelling. Baseline wander correction is also implemented inside the data path. A dedicated 7-tap FFE is employed for the CDR path to achieve lower latency timing recovery and allow independent optimization of the digital equalization. After the FFE, the timing error detector (TED) is generated and a 2nd-order loop filter drives the phase interpolator inside the RX clock path. All filters are automatically adapted with LMS engines. TI-ADC gain, offset and skew calibrations are also driven by DSP. With the MCU, RX and TX training are implemented in firmware to co-optimize the analog front-end and DSP to achieve high performance and low power consumption. Noise measurement, channel estimation and EOM features are also supported by DSP.

Figure 6.2.4 shows the TX block diagram. The 6-tap FFE is operated at 1/40-rate for pre-equalization supporting both NRZ and PAM-4 modulations, the main cursor location can be programmed for flexible pre- and post- emphasis configurability. A 40:8 MUX serializes the FIR output to 1/8 rate, the binary to thermometer encoder of the driver DAC and 1UI data staggering are also implemented in this block to relax timing closure in later stages. The 8:4 MUX serializes the data to 1/4 rate, and it also works as a re-timing stage to avoid additional DFFs for power consumption reduction. The final stage is an SST 7.5b DAC that is segmented into 3.5b thermometer MSBs and 4 binary LSBs. Each DAC slice has a 4:1 MUX that serializes data to 56GBaud. The SST switch size determines the TX power consumption and also impacts the DAC linearity and SNDR. The ratio of the SST switch to poly resistance is chosen as 1:1 to balance this trade-off. Programmable tail devices are employed for impedance calibration and temperature tracking. The output T-coil extends the bandwidth and improves the return loss. The 14GHz differential clock from the PLL is passed through delay stages to create 4 phase clocks with 90-degree separation. 1UI pulses with 25% duty cycle clocks are generated for the 4:1 MUX inside DAC driver. The duty cycle and quadrature error are detected based on the 1UI pulses for duty cycle correction and delay adjustment. The step size of DCC and adjustable delay are 0.1% and 70fs respectively. The TX DAC driver and clock path are powered from a 1.0V supply with LDOs. The whole TX achieves 1.1pJ/b with full rate including TX FIR.

The wireline transceiver is fabricated in a 5nm CMOS process, the TX eye diagram is shown in Fig. 6.2.5 with PRBS-13 pattern at 106.25Gb/s, the DAC driver achieves >36dB SNDR and >96% RLM. Figure 6.2.6 shows 138fs_{rms} jitter for a clock pattern with a 4MHz 1st-order CDR filter. The measured BER with different channel loss is listed in Fig. 6.2.5 at 106.25Gb/s, a BER of 1e-5 can be achieved with channel loss of 51.5dB. Figure 6.2.5 also shows JTOL and ITOL test results with the compliance testing setup. The transceiver passed the 100GBASE-KR spec across PVT. The single lane power consumption with long-reach 112Gb/s is 504mW including DSP, which corresponds to 4.5pJ/b. Figure 6.2.6 summarizes the transceiver performance and its comparison with recently published works. A die photo of the quad macro is shown in Figure 6.2.7.

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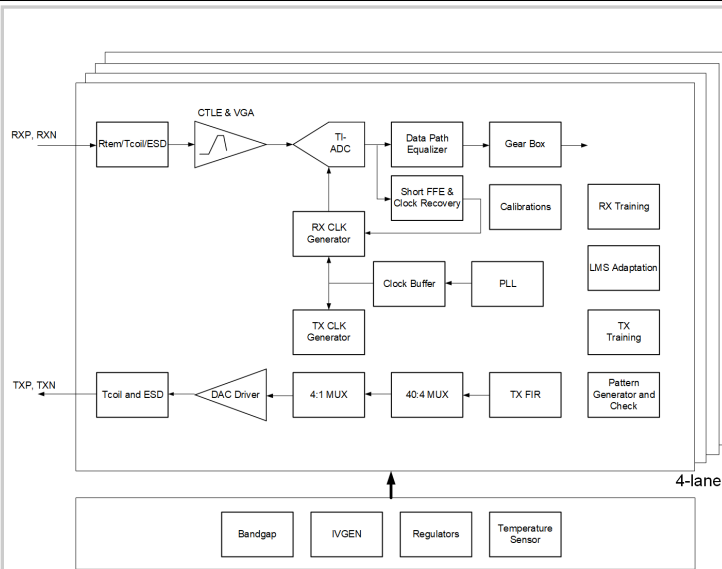


Figure 6.2.1: 4-Lane SerDes macro top level block diagram.

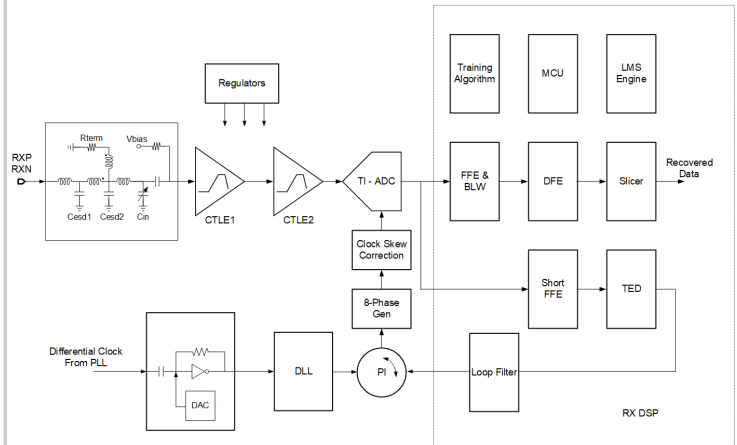


Figure 6.2.2: RX block diagram.

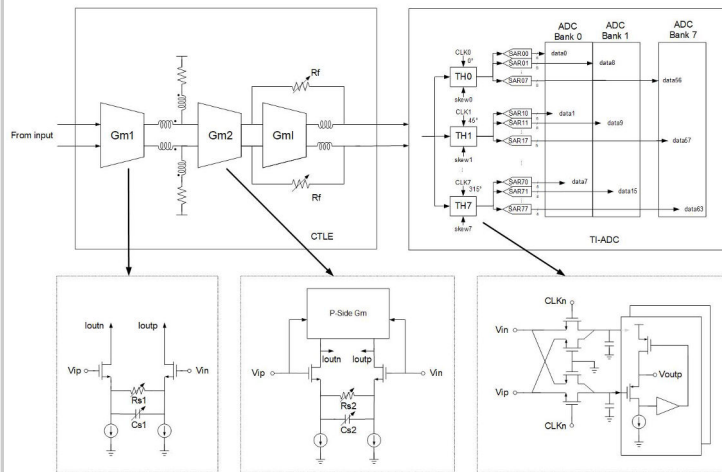


Figure 6.2.3: Architecture and circuits of CTLE and TI-ADC.

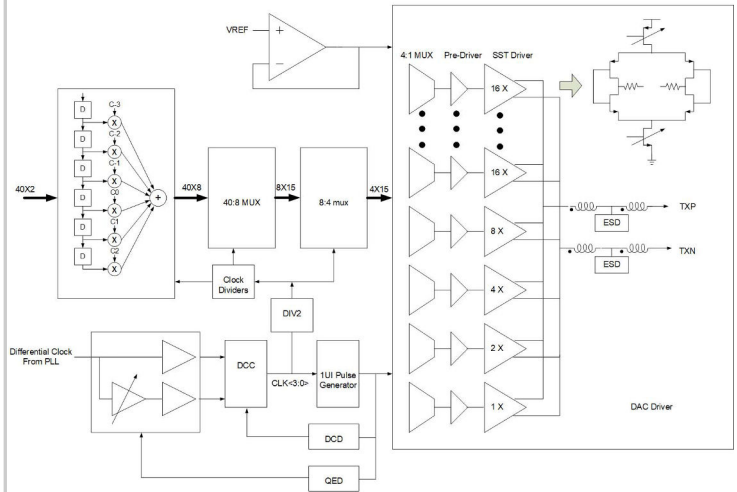


Figure 6.2.4: TX architecture and circuits.

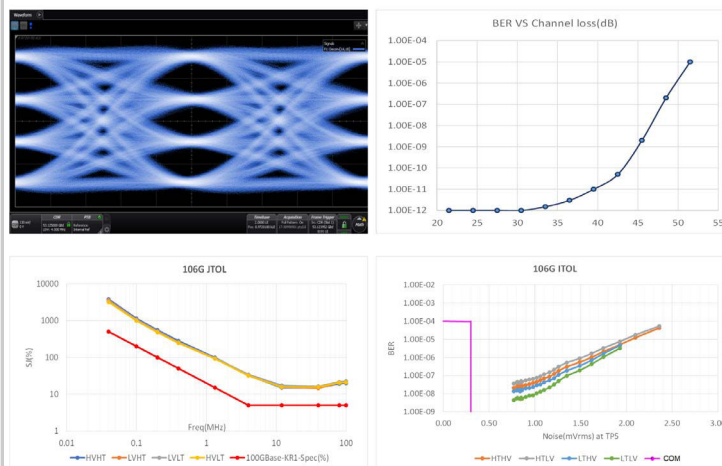
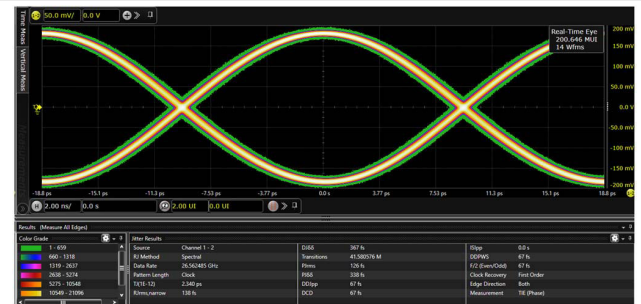


Figure 6.2.5: Measured TX full-rate eye diagram, BER change with channel loss, JTOL and ITOL.



	[1]	[2]	[3]	[4]	[5]	This Work
Technology	7nm	7nm	7nm	7nm	7nm	5nm
Data Rate (Gb/s)	112	112	112	112	112	112
Architecture	ADC/DSP	ADC/DSP	ADC/DSP	ADC/DSP	ADC/DSP	ADC/DSP
Supply Voltages (V)	0.88/1.2/1.5	0.85/1.2	0.75/0.9/1.2	0.875/0.8/1.0/1.2	0.65/0.94/1.15	0.75/1.0
BER/Loss @ Nyquist	1e-8	5e-7	1e-9	1e-10	2e-7	1e-9
	37.5 dB @ 28 GHz	38.9 dB @ 28 GHz	26 dB @ 26.5625 GHz	38 dB @ 28 GHz	41.5 dB @ 28 GHz	40 dB @ 28 GHz
RX Equalizer	CTLE	CTLE	CTLE	CTLE	CTLE	CTLE
	31-Tap FFE	24-Tap FFE	32-Tap FFE	25-Tap FFE	N/A	30-Tap FFE
RX SNDR (dB)	N/A	34.3	N/A	N/A	35	36
TX Arch	CML	7b SST	7b SST	7b SST+CML	7b CML	7.5b SST
TX Swing	4-Tap FFE	6-Tap FFE	8-Tap FFE	4-Tap FFE	4-Tap FFE	6-Tap FFE
Power/Lane (mW)	0.93	0.65	N/A	1.2	1	0.9
	602 (analog)	460 (analog)	921	662	729	504
Area (mm ²)/Lane	0.4 (analog)	0.385 (analog)	0.8188 (analog)	0.531 (analog)	0.92 (analog+Digital)	0.49 (analog+Digital)

Figure 6.2.6: Performance summary and comparison table.

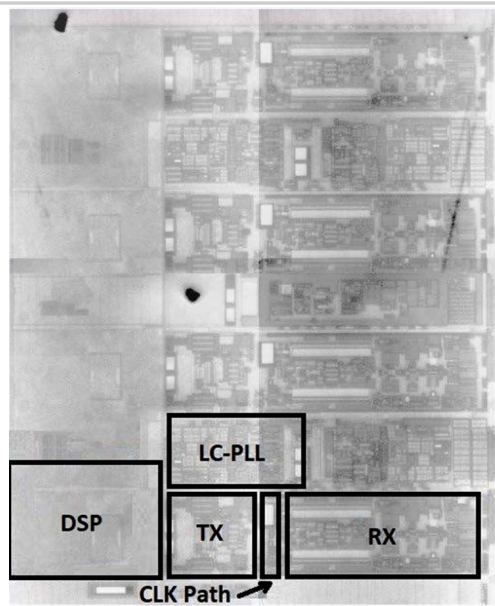


Figure 6.2.7: Die micrograph of the 4-Lane Macro.