Area Optimization of the Feed-Forward Equalizer for ADC-Based High-Speed Wireline Receiver Using Channel Characteristics

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***Abstract*—In high-speed serial link, the analog-digital converter (ADC)-based receiver (RX) architecture has been widely applied with 4-level pulse amplitude modulation (PAM-4) for $>$ 56 Gb/s/lane. While ADC-based RXs exhibit strong equalization capability, the feed-forward equalizer (FFE) in its digital signal processor (DSP) occupies a large area due to the large number of multipliers required to implement the parallel finite impulse response (FIR) filter. In this work, we explore the required number of bits for the FFE coefficients depending on the tap position given a chip-to-chip channel profile. By proper bit-level optimization of the FFE multipliers, 42 % of the FFE area could be saved for the twelve largest FFE tap values as compared to the case where the same-sized FFE multipliers are considered for a channel exhibiting 28 dB of loss at 28 GHz.**

***Index Terms*—Serial link, SerDes, wireline receiver, PAM-4, feed-forward equalizer, ADC-based receiver.**

I. Introduction

The exponential growth of data traffic in data center and supercomputing platforms demand an ever-increasing per-lane data rate of serial data transceivers (TRX) while limiting their power consumption [1]–[7]. Recently, analog-digital converter (ADC)-based receiver architecture with 4-level pulse amplitude modulation (PAM-4) has become popular in high-speed wireline TRX [8]–[11]. While digital signal processor (DSP) equalizers including a multi-tap feed-forward equalizer (FFE) and a single-tap decision-feedback equalizer (DFE) provide strong equalization performance, the FFE can occupy a significant portion of the receiver (RX) DSP area depending on the designed number of FFE taps. In this work, we study the area of the RX FFE with a tap-dependent coefficient width given the channel profile and the bit error rate (BER) target for chip-to-chip wireline communication.

II. System Model

Fig. 1 shows the overall block diagram of an ADC-DSP-based RX. Analog front-end consisting of continuous-time linear equalizer (CTLE) and variable gain amplifier (VGA) partially equalizes the incoming PAM-4 signal and adjusts its overall amplitude to use the ADC's input dynamic range most efficiently. The time-interleaved ADC (TI-ADC) digitizes the analog signal, then the FFE performs linear equalization in the discrete-time with discrete amplitude. The DFE typically performs a one-tap nonlinear equalization enhancing the signal-to-noise ratio (SNR) of the digitized signal. The FFE and the DFE taps are typically adapted based on the least mean-square (LMS) algorithm, and the TI-ADC's optimal sampling phase is updated by the clock-data-recovery (CDR) block and the phase rotator (or phase interpolator).

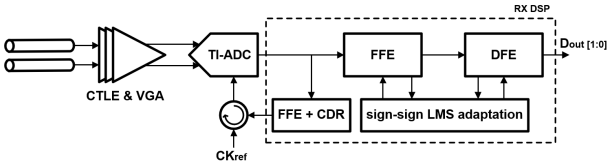


Fig. 1: Overall block diagram of the ADC-DSP-based RX.

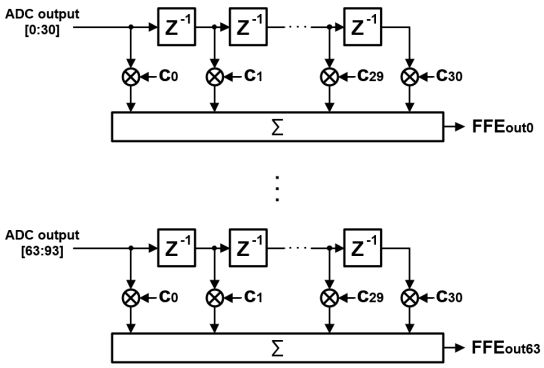


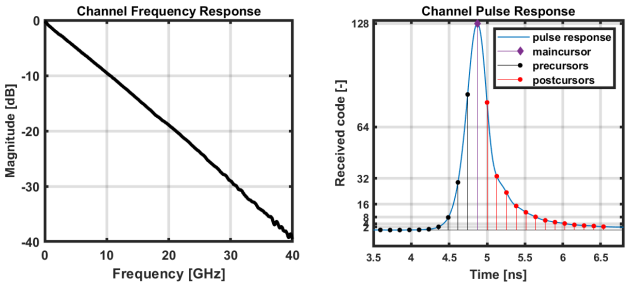
Fig. 2: A 31-tap FFE in the RX DSP based on the 64-way parallel FIR filter.

The structure of the digital FFE is shown in Fig. 2. The underlying structure is simply a parallel digital finite impulse response (FIR) filter, where each of the parallel paths is composed of an array of coefficient multipliers and a summer.

III. Digital FFE Area Optimization

The multiplier corresponding to each FFE tap does not have to be the same one another as the inter-symbol interference (ISI) cursor values have a large variation. For example, when

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(a) (b)

Fig. 3: Measured channel frequency response [12] (a), and the corresponding pulse response with 56 GBaud (b).

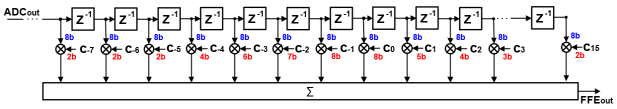
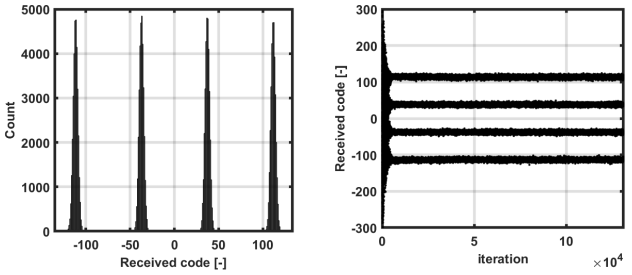


Fig. 4: Per-tap bit-width-optimized FFE multipliers (only 7 post-cursors, the main cursor, and 3 pre-cursors are shown out of 31 taps).



(a) (b)

Fig. 5: Histogram of the equalized PAM-4 symbols (a), equalized samples in the time-domain after FFE (b).

communicating through a channel of which frequency response is shown in Fig. 3(a), the corresponding pulse response shown in Fig. 3(b) has its ISI values ranging from below 2 to nearly 90 in 7-bit digital code depending on the cursor position. As point-to-point wireline channels typically have a relatively smooth low-pass filter nature, the maximum and minimum tap values at each tap position (or index) can be statistically determined given a set of measured channels. Considering a particular channel pulse response seen by the ADC shown in Fig. 3(b), the 4^{th} post-cursors and the 2^{nd} pre-cursors can be represented with a 4-bit resolution instead of the 8-bit of input resolution, as can be seen in Fig. 4. Similarly, the FFE tap coefficients that are sure to be smaller than a certain value in magnitude, they can be expressed with a just sufficient number of binary bits to save silicon area.

IV. Simulation Results

With the per-tap bit-width optimization, the FFE coefficients' bit-width for 7 post-cursors and 3 pre-cursors can be reduced to $[b_{-7}\, b_{-6} \cdots b_{-1}\, b_0\, b_1 \cdots b_3] = [2\,2\,2\,4\,6\,7\,8\,8\,5\,4\,3]$ instead of all-8-bit coefficients for the channel shown in Fig. 3 with 112 Gb/s PAM-4 (56 GBaud). This particular example shows a 42 % area reduction to the FFE multipliers for the twelve largest FFE tap values without sacrificing the BER of the FFE-equalized signal. The histogram and the time-domain samples of the equalized PAM-4 symbols with the reduced-bit FFE coefficients are shown in Fig. 5(a) and Fig. 5(b), respectively.

V. Discussion

As the precondition of the proposed technique is a smooth channel frequency response, the proposed scheme may have a narrow range of applications. However, when the impedance discontinuity is well-controlled in chip-to-chip interfaces, a significant area and power saving can be expected. In addition, far-end reflective post-cursors can be handled by floating FFE taps with their bit-width determined also based on the statistical optimization. Even when the channel frequency response has multiple ripples, the proposed technique can still be applied with margin bits at the cost of less aggressive optimization.

VI. Conclusion

In this work, we proposed an FFE area minimization technique based on the statistical per-tap coefficients' bit-width optimization for ADC-DSP-based RX. The proposed technique uses the channel loss profile of a chip-to-chip communication link to determine the maximum bit-width reduction for each FFE tap. Simulation results show that the FFE area for the twelve largest taps could be reduced by 42 % as compared to the case without any FFE coefficients' bit-width optimization for a channel exhibiting 28 dB effective loss seen by the ADC at Nyquist.

VII. Acknowledgment

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References

[1] Y. Frans *et al.*, "A 56-Gb/s PAM4 wireline transceiver using a 32-way time-interleaved SAR ADC in 16-nm FinFET," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 4, pp. 1101–1110, April 2017

[2] T. Ali *et al.*, "A 180mW 56Gb/s DSP-based transceiver for high-density IOs in data center switches in 7nm FinFET technology," *IEEE ISSCC Dig. Tech. Papers,* Feb. 2019, pp 118–120.

[3] Z. Guo *et al.*, "A 112.5 Gb/s ADC-DSP-based PAM-4 long-reach transceiver with >50dB channel loss in 5nm FinFET," *IEEE ISSCC Dig. Tech. Papers,* Feb. 2022, pp 116–118.

[4] J. Im *et al.*, "A 112Gb/s PAM-4 long-reach wireline transceiver using a 36-way time-interleaved SAR-ADC and inverter-based RX analog front-end in 7nm FinFET," *IEEE ISSCC Dig. Tech. Papers,* Feb. 2020, pp 116–118.

[5] Y. Segal *et al.*, "A 1.41pJ/b 224Gb/s PAM-4 SerDes receiver with 31dB loss compensation," *IEEE Journal of Solid-State Circuits,* vol. 58, no. 1, pp. 8-18, Jan 2023.

[6] G. Kim, "Design space exploration of single-lane OFDM-based serial links for high-speed wireline communications," *IEEE Open Journal of Circuits and Systems (OJCAS),* vol. 3, pp. 134–146, 2022.

[7] G. Kim *et al.*, "A 161mW 56Gb/s ADC-based discrete multitone wireline receiver data-path in 14nm FinFET," *IEEE J. Solid-State Circuits,* vol. 55, no. 1, pp. 38–48, 2020.

[8] P. Mishra *et al.*, "A 112Gb/s ADC-DSP-based PAM-4 transceiver for long-reach applications with >40dB channel loss in 7nm FinFET," *IEEE ISSCC Dig. Tech. Papers,* Feb. 2021, pp 138–140.

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[9] S. Kiran *et al.*, "A 52-Gb/s ADC-based PAM-4 receiver with comparator-assisted 2-bit/stage SAR ADC and partially unrolled DFE in 65-nm CMOS," *IEEE J. Solid-State Circuits,* vol. 54, no. 3, pp. 659-671, 2019.
[10] A. Roshan-Zamir *et al.*, "A 56-Gb/s PAM4 receiver with low-overhead techniques for threshold and edge-based DFE FIR- and IIR-tap adaptation in 65-nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 54, no. 3, pp. 672–684, March 2019
[11] G. Kim *et al.*, "A 4.8pJ/b 56Gb/s ADC-based PAM-4 wireline receiver data-path with cyclic prefix in 14nm FinFET," *Proc. of IEEE Asian Solid-State Circuits Conf. (ASSCC),* Nov. 2019, pp. 239–240.
[12] "IEEE P802.3ck Task Force—Tools and Channels." Accessed: 2019. [Online]. Available: http://www.ieee802.org/3/ck/public/tools/index.html
[13] J. Campello, "Optimal Discrete Bit Loading for Multicarrier Modulation Systlems," *IEEE International Symposium on Information Theory,* Aug. 1998, pp 193–.

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