

Dual-Band CMOS LNA for Ku-Band Applications

Arpit Tomar

Dept. of Electronics & Comm. Eng.
GCET, Gr. Noida, India
arpittomar801@gmail.com

Deepak

Dept. of Electronics & Comm. Eng.
GCET, Gr. Noida, India
deepakstrange8011@gmail.com

Aman Kumar

Dept. of Electronics & Comm. Eng.
GCET, Gr. Noida, India
amankumar5hit@gmail.com

Aman Yogi

Dept. of Electronics & Comm. Eng.
GCET, Gr. Noida, India
amanyogi842@gmail.com

Mr. Ravi

Dept. of Electronics & Comm. Eng.
GCET, Gr. Noida, India
ravi987@gmail.com

Abstract- In this work presents the schematic diagram of a LNA which represents a 90 nm CMOS technology. The low-noise amplifier (LNA) is design for working Ku-band application. The certain matching is applied at the circuit's input and output to provide stability. The software was used to design the LNA is advanced design system (ADS). In this study, the suggested LNA incorporated a source degeneration, resistive shunt feedback, cascode structure, input/output matching and cascode topologies. It works at two frequencies, 14 GHz and 16 GHz. In this LNA, the whole circuit power supply is 1 V so that the power consumption should be minimum. It confers a high gain, stability, linearity, noise figure and S-parameters. The proposed LNA design delivers a high gain of 21.6 dB at 14 GHz and 17.4 dB at 16 GHz. Noise figure is observed 2.9 at 14 GHz and 3.3 at 16 GHz. The design also observed good input and output matching. The stability factor of the LNA is 1.1.

Keywords— Low-Noise Figure, CMOS, Forward Gain, S-Parameters, Impedance Matching, LNA.

I. INTRODUCTION

An amplifier designed primarily to enhance the power delivered to a load is known as a power amplifier. High-speed wireless communication is becoming increasingly accessible and in high demand. As a result, there is a growing need for larger bandwidth applications. However, to address smaller bandwidth requirements, RF (radio frequency) circuits must operate at lower frequencies. One critical component in this context is the LNA (Low Noise Amplifier). The LNA serves to mitigate feed-line losses that occur between the antenna and the receiver. Additionally, it extends the effective range of the receiver system.

CMOS low-noise amplifiers with low noise figure and high gain are the most critical and challenging components in Ku-band [1]. To amplify any weak signal Low Noise Amplifier is used and it also reduced the signal noise so that the signal will not descript. The wireless communication systems often employ LNAs to enhances the quality of intercepted signal. Circuit design techniques and topologies have a considerable impact on LNA performance [2].

Particularly in satellite communications and 5G networks, a LNA is an indispensable element of radio frequency system. To Amplifying weak signals is the main function of LNAs which received from antennas with minimal noise introduction [1][2][3]. The function of these amplifiers is crucial in preserving the sensitiveness of the system as a whole [4,5] and high SNR (signal-to-noise ratio).

A range of methodologies, including cascading, feedback, and source-drain coupled line (SDCL), are utilized in low-pass filters (LNAs) to augment gain and diminish noise figure, thereby facilitating broad bandwidth operation at peak efficiency. LNAs are commonly installed at the input terminals of receivers in order to efficiently amplify incoming signals. Achieving optimal impedance matching, gain and noise figure are all design considerations for LNAs. As fundamental components of RF systems, LNAs are indispensable for the reception and processing of signals.

This study presents a CMOS LNA that operates at two frequencies, 14 GHz and 16 GHz. It is there at the receiver's front end. Section II of this publication reviews previous studies on a range of LNAs. section III represents the design topologies which are used in this research and how that topologies are beneficial in designing a sustained LNA. A circuit description of the proposed LNA's design is provided in Section IV. The simulation findings and their explanation are described in Section V. Additionally, Section VI contains the paper's conclusion.

The proposed work presents a CMOS LNA used at the receiver side and working at the two frequencies (14 GHz and 16 GHz). Section II contains the related previously research work on LNAs. LNA topologies are describe in Section III. In Section IV, the proposed LNA circuit design is described. Section V describes and explains the simulation results. And Section VI provides an explanation of this paper's conclusion.

II. RELATED WORK

In [2] there are total four techniques are used to achieve minimum consumption of power for wireless sensor network, using common source in cascode & cascode, self-biased inverters and last forward body biased, negative feedback of capacitor, fabricated in 180-nm technology, operate in 2.4 GHz with 10.1 dB gain, 2.88 dB NF & 0.6 V. The work in [3] on wideband LNA, resistive feedback and cascode arrangement [2, 3] using 90 nm achieving the good matching using pie-match I/P network, dissipates the 21.6 mW. In paper [4] the CMOS is fabricated with TSMC standard with the length 180-nm [2, 4] with operated on 14 mW and bring the peak gain at 24.2 GHz is 3.1dB and at 24.3 GHz the lowest NF is 3.9 dB, using common source two stage for noise and gain parameters. In paper [5] the author works on the 30 GHz frequency with 65 nm CMOS and focus on reducing difference between minimum noise figure (NF min) and noise figure (NF).

Circuit is two stage Low noise amplifier in cascode manner and it provide gain of 22.3 dB at 7 mW. This mainly works on 5 G millimeter wave band devices. In this source degeneration technique is used [5]. In work [6] the LNA is 180 nm wide and works in narrow band. It provides good input and output matching. The cascode arrangement is used for good NF. In the frequency range of 9.75 GHz to 10.25 GHz, the lowest recorded NF is 2.8 dB and the highest recorded gain is 15.69 dB. Common source topology is used, which aids in achieving low NF and high gain [2,6]. In paper [7] The LNA modeled in 65 nm [5,7] which works on wideband range of 110 GHz to 135 GHz. With a high gain of 29.11 dB, NF of less than 5.2 dB, and a 3 dB bandwidth of 20 GHz, this four-stage LNA offers both. Additionally, this LNA uses a 1.8 V source voltage and operates at 20 mW. The cascode structure is used in this four-stage LNA design, which is simulated in ADS, to obtain a flat gain response over a broad frequency range [11]. In work [8], 180 nm RF CMOS technology is used to implement the CMOS LNA on the Ku-band for phased array applications. It provides highest power gain at 17.5 GHz is 16.8 dB and minimum NF at 17 GHz is 4.5 dB under supply of 1.8V. These all parameter increase the Q-factor Work in [9] is on ultra-wide band with 3.1-10.6 GHz with the output of 9.7dB with 4.5-5.1 dB NF with consumption of 20mW and area occupational is 0.59 mm². The LNA in [10] is work with 30-50 GHz and GaAs or In PHEMT used for the astrological research, carbon chain evolution & observing generation of galaxy, TCMS fabricated in 90-nm and uses current reuse technology for boosting high frequency, operated in Q-Ban, operate at 1.4 V V_{DD}, achieved 20.5 dB gain with 4.2 dB NF, common source technology is used.

III. LNA TOPOLOGIES

The topologies of LNA (Low-noise amplifier) rely on varied configuration of its biasing network, the passive-components and amplifying device. Varied circuit topologies provide various levels of power, forward gain, linearity and NF. The suggested circuit designed by different topologies including as:

A. Cascode

The topology most frequently used to create amplifier circuits is the cascode scheme. The Miller effect is lessened by the cascode architecture. [2,5]. A respectable reverse isolation is provided by the similar suppression of the effects of low output impedance.

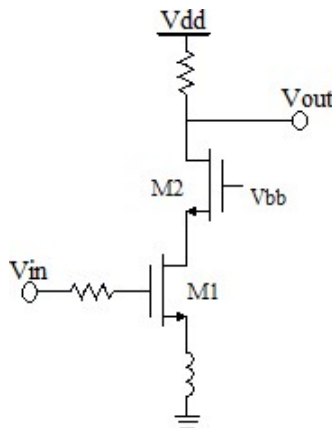


Fig. 1. Cascode Structure

Having a good isolation helps to attain better stability. By using this topology in the circuit, the whole gain will increase and also help to maintain low noise figure.

A common-source amplifier and a common-gate amplifier are connected in series in a cascode LNA. Compared to a conventional single-stage LNA, this configuration offers a number of benefits [9].

B. Resistive Shunt Feedback

Resistive shunt feedback technique is commonly used in the amplifier circuits. By using this in the circuit, it will increase the bandwidth of LNA [3,9]. In the circuit R1 and C2 is connected in feedback of the M1 CMOS which help to provides less noise figure and stable circuit. It uses a cascode design with resistive shunt feedback between gate and drain. The circuit design is shown in Fig. 2.

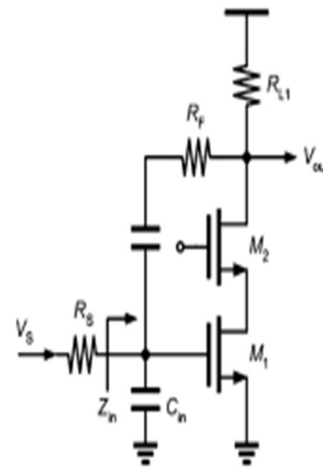


Fig. 2. Resistive shunt feedback

In the Fig. 4 negative feedback capacitor is directed connected to drain to gate terminal of M3. The forward gain, noise figure, and impedance matching of the LNA could all be adjusted with the use of the source inductance negative feedback with cascode circuit, as illustrated in Fig. 3.

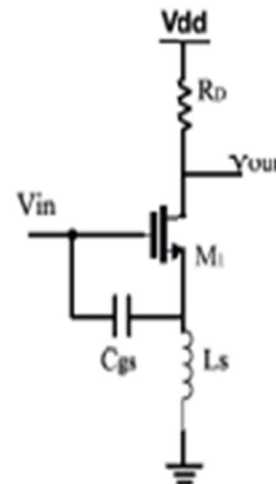


Fig. 3. Negative feedback

IV. CIRCUIT DESCRIPTION

While designing a LNA schematic, many key components, like inductors, an bias resistors used for good gain, stability, input/output impedance matching and impedance matching network. The LNA circuit's particular configuration depends upon the several parameters that includes forward gain, linearity, power consumption, noise figure, stability, input and output matching. The proposed LNA circuit shown in Fig.4. The circuit contains two stages and three transistors used for design the LNA. The length of every CMOS is 90 nm and the width of M1 is 21 nm. First stage has a transistor which is cascade to second stage which has two transistor cascode to each other. The cascade technology is used to improve the gain of the LNA. In second stage, , cascode schematic, a capacitor is used as source inductance negative feedback with gain, impedance matching and also noise figure of the Low Noise Figure (LNA) could be optimized [3]. And a source-degradation inductor L1 is added to increase the stability as well as the linearity of the circuit design. And a Resistive shunt feedback with a series combination of resistor and capacitor is connected to gate of the M3 CMOS which is shown in Fig. 4. In second stage, the width of M2 and M3 are 50 μm and 70 μm , while channel length is 90-nm. For minimize the power consumption, whole circuit has 1V power supply. While cascaded of first stage and second stage a network of lumped components C3, C4 and L4 is used to connect both stages. In second stage, a resistive shunt feedback, series combination of resistance and capacitor is applied at the terminal of M2 transistor and a 1V supply voltage is provided at the gate terminal. At the M3 transistor a negative-feedback of capacitor is direct connected to the source to gate terminal that help to provide low noise figure and the high gain. A source degeneration inductor L1 is connected at the M3 transistor so that the noise figure remains low. The proposed LNA design works on 90 nm CMOS technology.

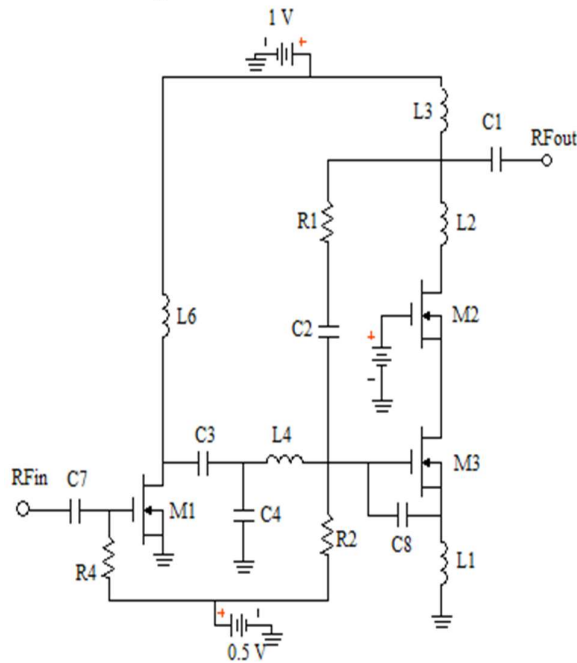


Fig. 4. Proposed Circuit Design

The input matching is done by a L matching network, which uses lumped components of the series combination of R4 and C7. This helps to keep the noise figure low. RF choke is

connected at the output which generate good output matching. L3 and C1 combined are utilized as an RF choke and for RF tuning. The circuit uses a 1V power source to maintain its low power usage.

V. RESULT & DISCUSSION

The amplifier's capability to increase the level of the input signal is because the receiver can perfectly gain and measure its gain. Alternatively, it may be considered the ratio of electrical output to the input.

Gain of an LNA circuit is important parameter that determine the performance of the LNA. It represent the strength of the receiver signal. A high gain represent the signal strength that makes the signal easy to detect.

The unit of Gain is calculated in decibels (dB) so the values for LNA gain are in between of 10 to 30 dB. In this article, the LNA was created utilizing a 1V capacity supply, and the gain generated 17.4 dB at 16.5 GHz and 21.6 dB at 14.3 GHz, as shown in Fig.4.

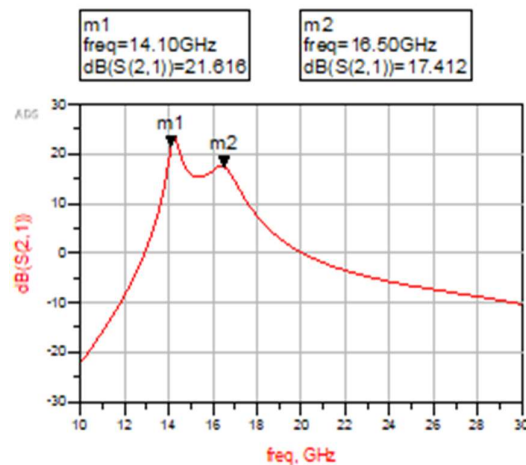


Fig. 5. Forward Gain S(2,1)

S-parameters : also known as Smatrix or scattering are the most important parameter to analysis the LNA circuit. S-parameter shows forward gain, output reflection coefficient, input reflection coefficient and reverse gain. The reflection coefficient S(2,2) is illustrated in figure 5. It also describe good output matching. Its value is calculated as -9.8 dB at 14.4 GHz.

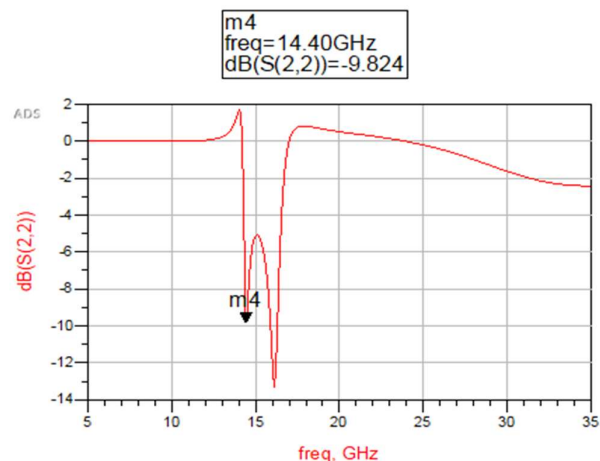


Fig. 6. Reflection Coefficient S(2,2)

Reflection Coefficient $S(1,1)$ of -4.4 dB are obtained at 14.3GHz, as shown in Fig. 6.

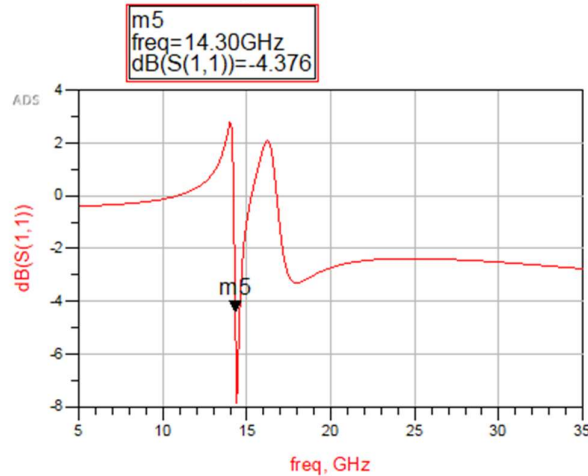


Fig. 6. Input Reflection Coefficient $S(1,1)$

Fig. 7 provides proof of the simulated $S(1,2)$, sometimes referred to as isolation or reverse gain, which is seen to be -20.1 dB at 14.3 GHz.

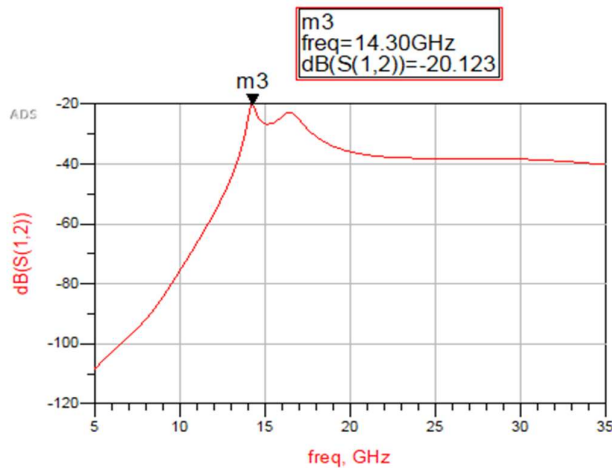


Fig. 7. Reverse Gain $S(1,2)$

Noise Figure in a Low Noise Amplifier (LNA) represents the ratio of the total noise power at the output to the noise generated at the input.

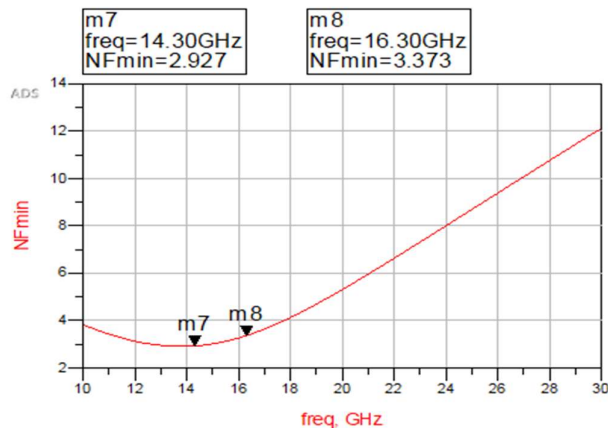


Fig. 8. Noise Figure

Generally, lower noise figures indicate better performance for radio amplifiers. An effective LNA should have a low noise figure, which implies reduced noise. In the specific circuit mentioned, the noise figure (NF) was 2.9 at 14.3 GHz and 3.3 at 16.3 GHz, which is acceptable for Ku-band applications

Stability Factor of LNA circuit is shown in Fig. 9. Its value is at 14.3 GHz and at 1.1. The values are higher in number 1, therefore it may be said that the LNA shows fixed traits.

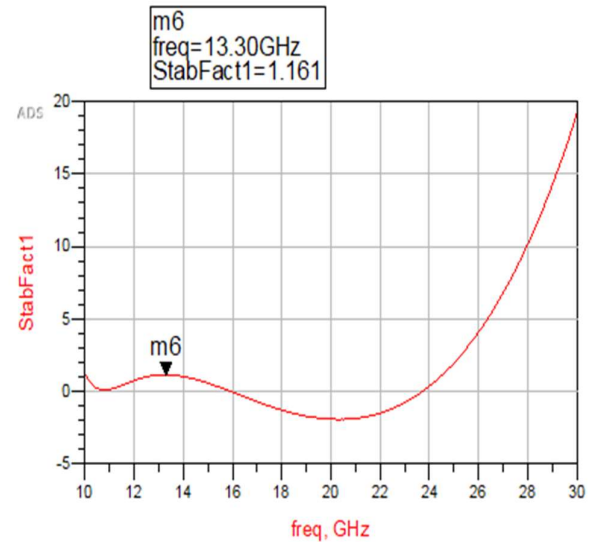


Fig. 9. Stability Factor (K)

The simulation result of the proposed LNA circuit design are compared with other research paper work in Table I.

TABLE I. Comparative analysis of LNAs

REF.	Freq. (GHz)	Gain (dB)	NF (dB)	Power (mW)	TECH.
THIS WORK	14.3 16.3	23.62 17.72	2.90 3.3	10.7	90 nm
[1]	17.5	18	3.6	12.6	180 nm
[2]	2.4	10.1	2.88	0.84	180 nm
[3]	3.1	10.48	2.92	21.6	90 nm
[7]	10	15.69	2.8	8.44	180 nm
[8]	16.4 19	13.6 16.8	4.5 5.2	66	180 nm
[9]	1.2-11.9	9.7	4.5-5.1	20	180 nm
[10]	25.5	20.5	4.2	10.1	90 nm
[11]	21 28	17.6 11.7	1.9 1.7	3.33	180 nm

VI. CONCLUSION

While designing LNA, many topologies and impedance matching is required to use in the circuit. The study depicted here gives a unique plan of 90 nm CMOS LNA circuit for Ku-Band. The two frequencies that the schematic is functional at are 14 GHz & 16 GHz. The supported low-noise amplifier (LNA) supplies over the top gain all through all frequency bands while at the same time keeping up high gain, great impedance matching and low noise figure. The circuit contain of two stages of CMOS transistor and contains three transistors. The proposed circuit consists of a cascode structure to connect two stages through network of lumped components. The provided gain of the LNA at 14 GHz is 21.6 dB and at 16 GHz is 17.4 dB. The generated noise figure is 2.9 at 14 GHz and 3.3 at 16 GHz. The circuit also generate output reflection coefficient ($S_{2,2}$) is -9.8d and input reflection coefficient ($S_{1,1}$) is -4.3dB. And the reverse gain of the paper is -20.1 dB at 14 GHz. The paper also describes the stability factor of LNA should be bigger than 1.

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