

The Design of Wideband LNAs in 45nm SiGe BiCMOS

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Abstract—This work presents the design of two low-noise amplifiers (LNAs) with variations in the second amplification stage to study trade-offs in gain, bandwidth, and linearity. Implemented in a 45nm SiGe BiCMOS process, the two designs achieved wideband gains (S21) from 16.2-55.0 GHz and 11.1-32.1 GHz with simultaneous broadband input matching (S11) bandwidths of 26.1-55.0 GHz and 11.6-33.4 GHz, respectively. The LNAs obtain a minimum noise figure (NF) of 3.4 dB and 2.3 dB, peak gains of 13.1 dB and 19.9 dB, and maximum IIP3s of 5.7 dBm and -4.7 dBm while using 18.0 mW and 14.4 mW of power from a 1.5V supply. These performance metrics enable record FoM performance when compared to both state-of-the-art CMOS and SiGe LNA designs.

Keywords—linearity, low-noise amplifier (LNA), mm-wave, noise figure, SiGe BiCMOS, wideband.

I. INTRODUCTION

There has been growing demand for RF front ends to provide both high gain and linearity in order to support spectrally-crowded 5G small cell wireless access nodes in the K/Ka band. Recent state-of-the-art LNA works have focused on wideband and power efficient multistage designs [1], or achieving simultaneous broad-band input matching and low-noise performance through three-winding transformers [2], with neither approach addressing linearity. Works focusing on high-linearity have used biasing structures [3] or a single-stage design [4]. However, both of these works suffer from low gain and narrow bandwidth. SiGe LNA designs have achieved high bandwidth and gain [5] through multi-stage gain staggering, as well as the highest power efficiency [6], but both works suffer from very low linearity.

This work presents the design of two wideband LNAs with variations in the second stage to study tradeoffs between achievable linearity and gain in a 45nm SiGe BiCMOS process [7]. Furthermore, to the author's best knowledge, the presented work achieves record FoM when compared to state-of-the-art high-linearity SiGe LNA designs.

II. SiGe BiCMOS TECHNOLOGY

The 45nm SiGe technology used in this work provides 10 metal layers and metal-insulator-metal (MiM) capacitors, as detailed in Fig. 1(a). The top-most metals M_{10} and M_9 were used for all interconnects with patterned M_1 shielding to achieve high Q for all interconnect at mm-wave frequencies. Fig. 1(b) shows a 3D layout of the bipolar device that uses a C-B-E-B-E-B-C orientation due to its low noise figure from multiple base contacts. Metals M_1 to M_6 are routed straight up from the device terminals, while M_7 and M_8 were used

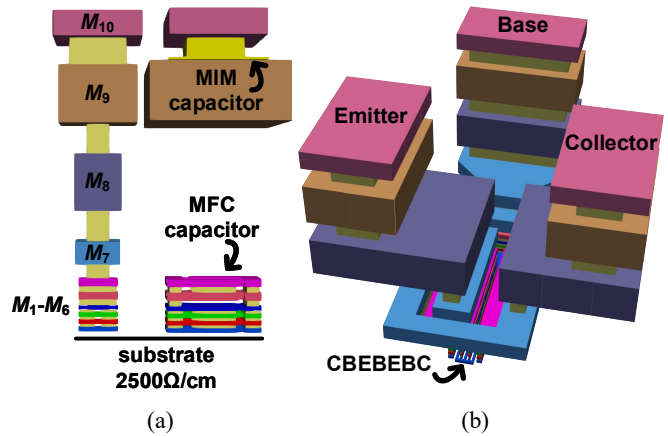


Fig. 1. 45nm SiGe BiCMOS process: (a) cross-section of metal back-end and (b) HBT device layout.

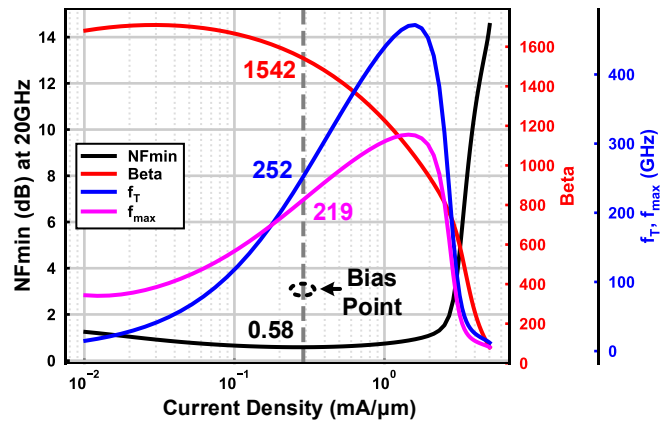


Fig. 2. Simulated NF_{min} , β , f_T , and f_{max} across current density.

to fan-out the terminals to reduce collector-emitter parasitics and improve isolation. The collector is wrapped around the device's perimeter to reduce collector resistance. The bipolar unit cell was EM simulated with the full metal stack-up from M_1 to M_{10} achieving a post-EM peak f_T of 460 GHz, as shown in Fig. 2. Furthermore, at a current density of 0.29 mA/ μ m the bias point for the NPN device was chosen for minimum achievable NF_{min} and it provides 90% of peak β , 54% of peak f_T , and 70% of peak f_{max} . This bias point simultaneously optimizes for low power, wide bandwidth, and low noise.

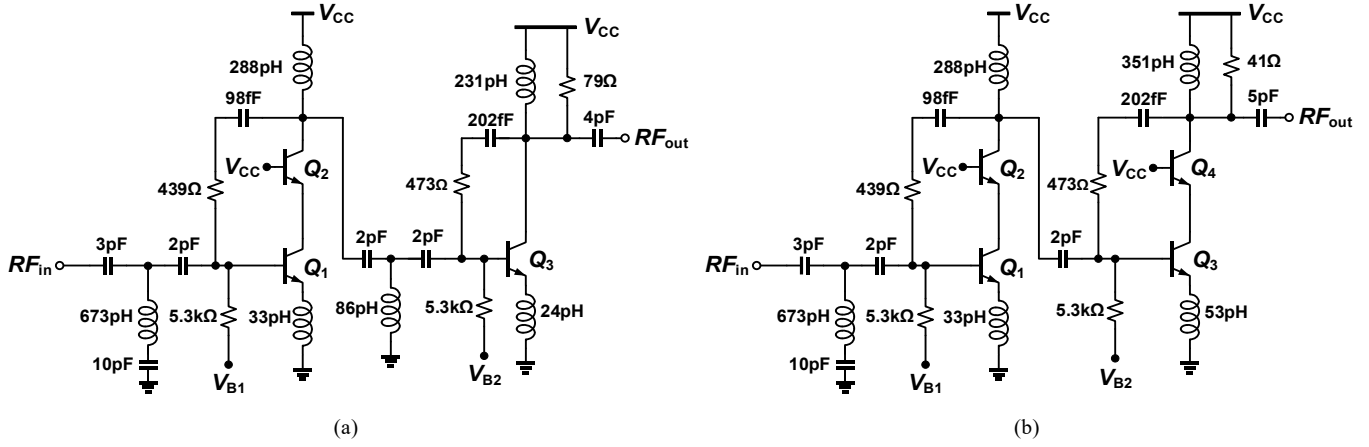


Fig. 3. Schematics of (a) LNA1 with wide bandwidth and high linearity and (b) LNA2 with wide bandwidth and high gain.

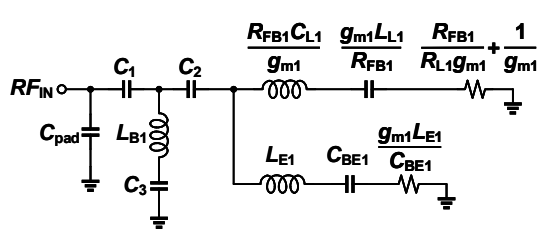


Fig. 4. Simplified input network derived from resistive feedback and inductive degeneration techniques.

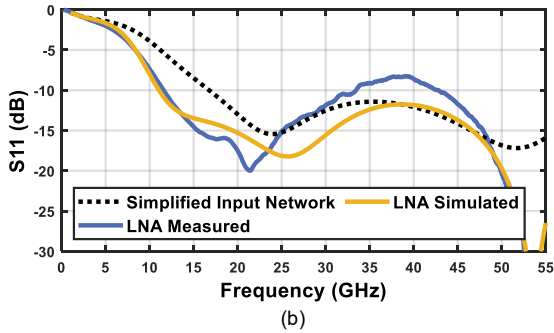
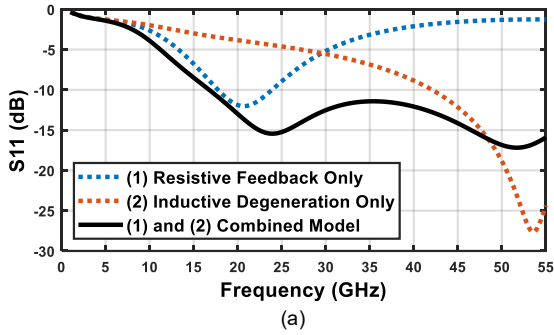


Fig. 5. Comparison of the (a) simplified input network matching simulation with (b) schematic and measurement results.

III. DESIGN TECHNIQUES

Schematics of the two LNAs are detailed in Fig. 3 with LNA1 utilizing a cascode first stage and common emitter

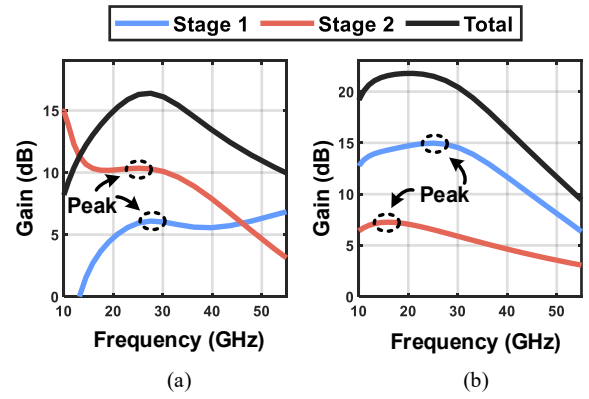


Fig. 6. Gain staggering simulations of (a) LNA1 and (b) LNA2.

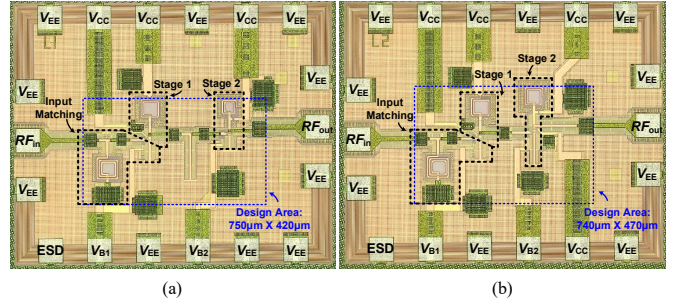


Fig. 7. Die micrographs of (a) LNA1 and (b) LNA2.

second stage, and LNA2 using cascode devices in both stages. Moreover, the cascode common-emitter design in Fig. 3(a) achieves high linearity due to the common-emitter stage providing a larger voltage headroom. The cascode-cascode design targets a high-gain response due to the cascode devices providing higher output resistance and hence gain at the expense of linearity. Given the SiGe technology, both LNAs uses 1.5V supply which dramatically improves the linearity of both LNA1 and LNA2 when compared to low voltage CMOS designs.

Resistive feedback and inductive degeneration are utilized to achieve wide input-matching bandwidth for both LNAs.

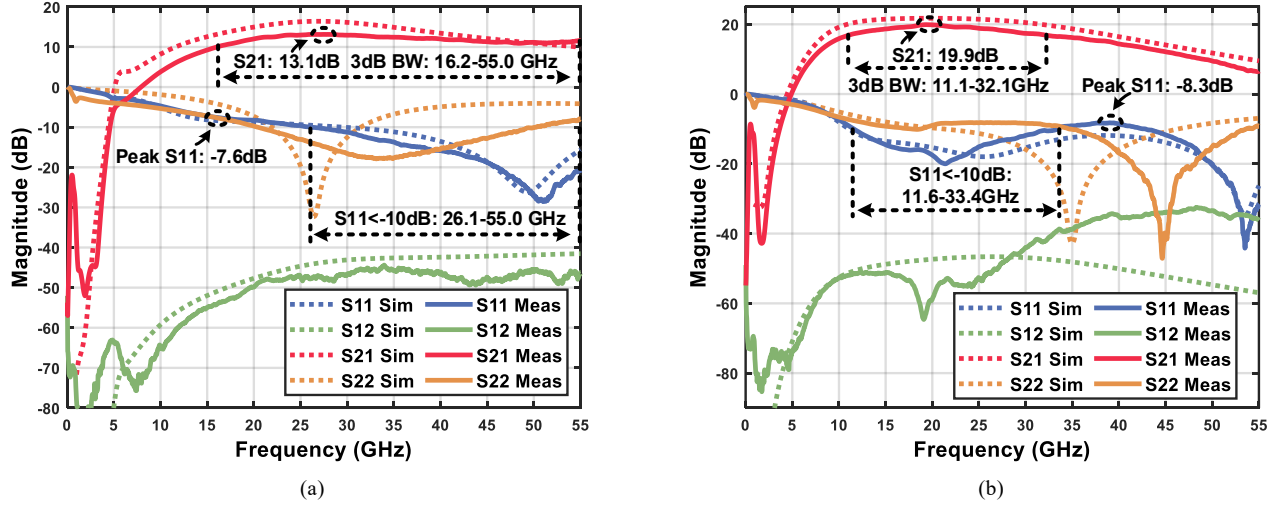


Fig. 8. Measured and simulated S-parameters of (a) LNA1 and (b) LNA2.

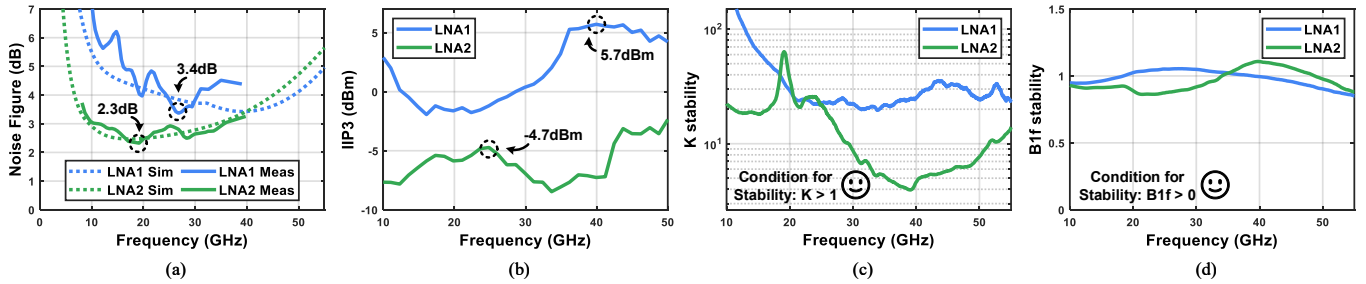


Fig. 9. Measured LNAs (a) noise figure, (b) linearity, and stability tests (c) Kf and (b) B1f.

Moreover, we simplify the input-network in a similar manner to [8] which allows us to decompose the input network into two resonant paths to create a simplified input-matching network as shown in Fig. 4. In Fig. 5(a) it is shown that at lower frequencies the resonant path from the feedback resistor to the first stage's output LC tank provides the match while at higher frequencies the resonant path from the inductive degeneration provides the match. By combining these two resonant paths a broadband input match is achieved. Moreover, in Fig. 5(b) the derived simplified input-matching network shows close matching between the simulated and measured S11 results.

To achieve a wideband gain response, the output LC tanks of each amplification stage are tuned to different frequency peaking values to stagger the gain. In Fig. 6 a simulation of the per-stage gain of each LNA details shows how the gain staggering was implemented to achieve a wideband response. All of the inductors used in this design were optimized to have a quality factor of at least 20 and a self-resonant frequency greater than 80 GHz.

IV. EXPERIMENTAL RESULTS

A micrograph of the two LNA designs are shown in Fig. 7 with LNA1 occupying 0.315 mm^2 and LNA2 occupying 0.347 mm^2 . The input and output GSG pads were probed with the DC pads wire-bonded. A Rohde & Schwarz ZVA67 was used

for S-parameter measurements and an NRP-Z57 was used for IIP3 measurements. An FSV40 and Pasternack PE85N1008 noise source were used for noise figure measurements. S-parameters of both LNAs are shown in Fig. 8 with LNA1 achieving an S21 3-dB bandwidth from 16.2-55.0 GHz and a peak gain of 13.1 dB with S11 below -10 dB from 26.1-55.0 GHz and a peak S11 of -7.6 dB at 16.2 GHz within the 3-dB bandwidth while consuming 18 mW of power. For LNA2, the measured S21 achieves a 3-dB bandwidth from 11.1-32.1 GHz and a peak gain of 19.9 dB with S11 falling below -10 dB across 11.6-33.4 GHz while consuming 14.4 mW of power. In Fig. 9(a) the measured noise figures for both LNAs are shown with LNA1 achieving a minimum NF of 3.4 dB and a LNA2 achieving minimum NF of 2.3 dB. Moreover, the measured NF for LNA1 shows more deviation due to its lower gain which affects NF measurement accuracy. The measured linearity (IIP3) of both designs is also detailed in Fig. 9(b) with LNA1 achieving a peak IIP3 of 5.7 dBm and LNA2 achieving a peak IIP3 of -4.7 dBm. In Fig. 9(c) and Fig. 9(d) both designs satisfy K and B1f stability factors across the measured spectrum.

Table I compares the performance of both LNAs against current state-of-the-art designs, high-linearity designs, and SiGe based LNA designs. These designs are compared with

Table I. WIDE-BAND LNA PERFORMANCE COMPARISON

Reference	This Work LNA1	This Work LNA2	[1]	[2]	[3]	[4]	[5]	[6]
Technology	45-nm SiGe	45-nm SiGe	28-nm CMOS	65-nm CMOS	28-nm CMOS	22-nm CMOS	90-nm SiGe	180-nm SiGe
3-dB Bandwidth (GHz)	16.2-55.0 (38.8)	11.1-32.1 (21.0)	19.5-62.5 (43.0)	28.1-48.1 (20.0)	21-34 (13)	19-34 (15)	10-110 (100) ^a	28.8-36.2 (7.4)
Peak Gain (dB)	13.1	19.9	18.4	21.5	8.6	12	25.5	18.0
NF (dB)	3.4-5.0	2.3-3.0	3.83-5.72	2.2-3.2	3.3-4.3	1.46-1.7 ^b	4.8-5.3	2.75-3.8
Peak IIP3 (dBm)	5.7	-4.7	-8.4 ^c	-7.6	12	3	-15 ^b	-23.4 ^c
Power (mW)	18.0	14.4	13.74	22	25.2	9.8	96	5.9
FoM ₁ (dB)	18.28	26.30	25.29	24.29	1.73	23.67	19.75	21.04
FoM ₂ (dB)	31.75	28.83	26.46	25.68	26.26	33.19	20.02	21.08

[^a]: Gain variation greater than 3-dB within the bandwidth

[^b]: Estimated from graph

[^c]: IIP₃ estimated from $P_{1dB} + 9.6dB$

two figures of merit (FoM):

$$FoM_1 = 20 \log_{10} \left(\frac{S_{21}[lin.] \times BW_{3dB}[GHz]}{P_{DC}[mW] \times (NF[lin.] - 1)} \right) \quad (1)$$

$$FoM_2 = 20 \log_{10} \left[\left(\frac{S_{21}[lin.] \times BW_{eff}[GHz]}{P_{DC}[mW] \times (NF[lin.] - 1)} \right) \times (1 + IIP_3[lin.]) \right] \quad (2)$$

The conventional FoM₁ accounts for peak gain, 3-dB bandwidth, power, and noise figure, while FoM₂ accounts for the same parameters but includes an IIP3 term in the numerator to reward wideband high-linearity designs.

Comparing LNA2 against current state-of-the-art designs [1] [2], a comparable bandwidth greater than 20 GHz, low NF, high gain, and low power is achieved while having higher linearity than both works. Comparing LNA1 against the high-linearity works [3] [4], a 3-dB bandwidth more than double that of the compared works is achieved with a higher peak gain. Moreover, the achieved IIP3 value of LNA1 falls between the two works. Comparing both LNAs against past SiGe LNA [5] [6], improvement in power and NF are achieved without sacrificing the gain and 3-dB bandwidth. When considering linearity using FoM₂, both LNA1 and LNA2 achieve the second and third highest performance while having significantly higher gain and bandwidth than [4]. Furthermore, LNA2 achieves the highest FoM₁ from all published works in Table I.

V. CONCLUSION

The design of two wideband mm-Wave LNAs implemented in a high f_T 45nm SiGe process was presented. The two architectures, a cascode + common emitter and cascode + cascode LNA, were implemented to study trade-offs between achievable operating bandwidth and linearity. Furthermore, it was found that by using a cascode + common-emitter architecture we can simultaneously achieve both high wideband gain and high linearity which has been historically difficult to do due to fundamental trade-offs between multi-stage gain staggering and linearity.

VI. ACKNOWLEDGMENTS

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