

Low-Power Deep-Submicron CMOS Adder Using Optimized Delay Universal Gates



J. Jeba Johannah, Reebea Korah, and G. Maria Kalavathy

Abstract Scaling down of CMOS technology requires vital reduction of leakage power in low-power applications. Power gating technique is generally employed in the standby mode to reduce static power consumption but it increases delay of the logic cells badly and the ultimate result of the circuit is besmirched to a great extent in deep submicron circuits. This paper utilizes feedback mechanism for reducing dynamic and static power during active and standby mode, respectively, and power gating technique is also engaged for further minimizing static power during standby mode. Novel optimal power gates such as NOT, NAND, NOR, and EX-OR are developed and simulations are done with 45 nm CMOS technology and 0.6 V supply voltage for the 32-bit ripple carry adder. Proposed adder using optimal power NAND gate accomplishes 46 percent reduction in dynamic power consumption and 84.3 percent reduction in static power consumption and 28.98 percent reduction in power delay product.

Keywords Delay · Dynamic power · Leakage power · Low power · Power gating · Power dissipation

1 Introduction

The prime concern of electronic portable device is to operate a device several hours without charging the battery. The increased usage of laptops and cellular phones make low power design a must. Static CMOS gates are very efficient since they are considered to dissipate zero power while it is idle. However, the number of transistors and

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clock frequencies increasing may lead to a sharp rise in power consumption. Moreover, scaling down of technology makes leakage power dissipation more significant compared to dynamic power.

Major components of power dissipation in CMOS circuits are static power and dynamic power dissipation [1]. The static power dissipation, mainly due to leakage current in CMOS circuit, has the following major components. One such component is subthreshold conduction through transistors which are turned off. This happens when the gate voltage of a transistor is less than threshold voltage and there is a voltage being applied between drain and source. The next one is due to gate oxide direct tunneling current. This leakage occurs through leaky oxide insulation from gate to substrate. Moreover, reverse biased current from reverse biased diodes formed between source and drain causes leakage in the junction. The last one is due to contention current in circuits. These leakage currents may flow both during active and standby mode of operation of the circuit. The amount of leakage through the above said components varies with the style of the circuit, the technology employed, and the temperature of the circuit. Scaling down of technology helps to accomplish higher density and lower power consumption. Moreover, supply voltage scaling tends to substantially increase subthreshold leakage current which is dominant in logic cells. Hence, this leakage current is a major problem for battery powered designs in deep submicron devices. This leakage current depends on gate to source voltage, the length of the transistor, and the temperature. Dynamic power dissipation, due to switching power and short circuit power, creates most of the power dissipation in CMOS circuits. Charging and discharging of the load capacitances of a CMOS VLSI circuit are the main cause for this power consumption. Scaling down of technology makes static power dissipation almost equal to that of dynamic power dissipation. Many of these portable devices function in the inactive mode for a extended time in comparison to the dynamic mode make the static power dissipation vital in these devices.

CMOS circuits in deep submicron VLSI utilizes two techniques, namely process level technique and circuit level technique, to lessen the subthreshold leakage current. By varying dimensions of MOS transistors, subthreshold leakage power can be decreased at the process level. By governing the voltages of MOS transistor terminals, leakage power can be reduced at the circuit level. In this presentation, subthreshold leakage power is minimized by using circuit-level techniques in the inactive mode and thereby to curtail total power dissipation.

Various design techniques have been employed so far to minimize leakage power in active and standby modes. Power gating technique had been adopted in standard cell designs to achieve high performance of the CMOS circuits [2]. Power gating technique cuts off power supply entirely from logic cells in sleep mode with the help of a switch. The switch can be implemented using one NMOS transistor/PMOS transistor connected in series with the NMOS transistors/PMOS transistors, respectively, in the logic block to create a power supply V_{DD} or a ground V_{SS} , which are virtual. These power gating transistors isolate cells from ground rail or supply rail or from both to break standby mode leakage in the circuit. But this technique requires alteration in CMOS technology in order to support both low-threshold and

high-threshold devices [3]. In addition, power gating reduces swing in voltage levels and hence the margin level in DC noise is lessened. Scaling down of power supply voltage makes all low threshold voltage transistors drive to go low which in turn makes transistors ON resistance to go high and this leads to usage of large sleep transistors and area overhead increases.

In this paper, we proposed a novel technique and synthesized NOT, NAND, and NOR gates to curtail power and to progress performance of these gates in nanoscale technology. The rest of the topics is structured as follows. Section 2 deals with review of well-known techniques. Section 3 shows design considerations of low-power VLSI and Sect. 4 presents the optimal delay gates to minimize active and dynamic power. Section 5 describes the implementation and simulation of the new methodologies. Conclusions are presented in Sect. 6.

2 Review of Well-Known Techniques

Keshavarzi et al. [4] suggested a technique called dynamic threshold CMOS which is advantageous in SOI devices which are partially depleted. Seta et al. [5] applied a method names as reverse body bias (RBB). This method lessens subthreshold conduction in the inactive mode but the NMOS and PMOS transistors threshold voltage are increased subsequently. Keshavarzi et al. [4] have also supposed that technology scaling may results in a sharp upsurge in junction current leakage with RBB technique. Kuroda et al. [6] proposed a technique known as variable threshold CMOS which could not be applied for deep submicron devices as a triple well technology or twin well technology need a substrate bias structures which are generated by itself. Wei et al. [7] recommended a technique called dual threshold CMOS in which finding which path is critical and then assigning different threshold voltages to the transistors which are in the critical path are tedious. Kawaguchi et al. [8] offered a method called as super cutoff CMOS power gating technique. The drawback here is that the desired bias to footers could be applied with the help of additional circuitry.

In multithreshold CMOS(MTCMOS) suggested by Mutoh et al. [9] make use of both header and footer transistors. Some of the present circuits make use of either a header or a footer. This structure curtails the needed area and the voltage drop in the dynamic mode. A header makes use of a PMOS transistor, and footer uses a NMOS transistor. Footer occupies less area as it has higher electron mobility in the active mode and it is customarily chosen. A header affects only pull-up transistors. Footer disturbs pull-down transistors. High threshold voltage transistors (HVT) are employed for both header and footer to cut off standby leakage and the logic circuit makes use of low-threshold devices. But this technique may not be helpful in for low supply voltages. Besides, area and delay become more in this technique. Tschanz et al. [10] presented a new method in which body biasing is employed along with power gating technique. The disadvantage is that it needed an additional circuitry. Shin et al. [2] suggested a technique called zigzag power gating. This technique requires a complicated power setup. Roy et al. [11] mentioned a gating technique to maintain

register state by maintaining a voltage across the power gated logic. This technique diminishes glitches and time for the circuit to respond to active mode back from sleep mode as valid logic outputs are maintained. Besides this, the area required for the circuit increases. Mistry et al. [12] offered subclock power gating technique that could be employed only for low-power applications in the dynamic mode. Zhang et al. [13] recommended multimode power switches for reducing power in the static mode. It has got large number of problems. One such problem is dynamic power consumption which is more in this technique. Secondly, this method suits only for static mode. Thirdly, digital power switches are used and hence this procedure cannot be implemented for analog circuits.

In this paper, we recommend a new procedure using power gating technique which restricts the negatives of the above system [13]. This one is appropriate for static mode of operation as well as dynamic mode of operation. We have combined RBB, power gating circuits with retention and added extra devices to boost the performance of the circuit, to diminish both dynamic and static power dissipation and to minimize the delay in the circuit.

3 CMOS VLSI Circuits Design Techniques

In CMOS VLSI circuits, power dissipation caused due to transition in input signal fluctuates as the square of the voltage applied. Hence, with supply voltage scaling, significant savings in power dissipation could be done.

The power gating structure consumes most power through sleep transistor. Attention should be given such that the power saved in the inactive mode through power gating should be made larger in comparison with the power used up by the power gating circuitry. Power gating technique could be classified as two types, namely coarse and fine grain power gating [14]. In the first type, a single transistor is shared by enormous number of circuits. This decreases the power and area consumption of the transistors used in the sleep mode. The drawback is that the same sleep transistor shared by any one of the circuits could be made inactive. However, in fine grain power gating, sleep transistor is distinct for each circuit and hence any particular circuit could be inactive as per requirement. Thus, the number of sleep transistor in the latter technique is much more than that of former technique. In fine grain power gating technique, in order to lessen leakage current, the size of sleep transistor should be made large which requires high threshold voltage transistors to be used as sleep transistors and the width of these sleep transistors should be made less in comparison with that of the total width in the down network. Moreover, the sleep transistors' size affects delay of the active mode circuit. The current passing through the pull-up/pull-down network leads to slowing down of logic circuits and the voltage drop across sleep transistor in the pull-up/pull-down network should be proportional to circuits total active leakage and dynamic current. Hence, the sleep transistor in the PMOS network should be large in order to have desirable voltage drop to compensate for the total current spent by the logic circuit.

The gate input is minimized from input voltage V_{DD} to $V_{DD} - \Delta V$ due to drop, ΔV , in voltage and the NMOS transistor threshold voltage is augmented due to body effect. These results in the current being minimized during discharge which in particular slackens down the output change from high to low signal. Designs in practical case need to have ΔV as small as possible so that delay due to sleep transistor is insignificant. The wake-up process implicates a huge current rushing through power gating transistors. This current results as a consequence of inductance from the power rails and can result in $L \cdot di/dt$ noise [2]. This is showed as V_{DD} variation when a PMOS transistor is engaged or as ground bounce when NMOS transistor is utilized.

It is frequently looked for to have identical propagation delays for rising inputs and inputs. By building the NMOS transistor ON resistance nearly equal to that of PMOS transistor ON resistance, propagation delays could be made equal to that of input. The performance can be made maximum by making the resistance of power gating transistor small and thus the size of the transistor large. Scaling down supply voltage causes the effective resistance of the standby mode transistor to increase vividly and hence sleep transistors with huge sizes are required.

In CMOS logic circuits, pull-up network transistors are attached to supply and pull-down transistors are attached to ground. An NMOS sleep transistor is suspended in parallel to header and it is attached to supply, V_{DD} to retain output value in the sleep mode and a PMOS transistor is joined to ground, in parallel to footer as retention transistor in parallel to footer network. When the basic transistors are switched off, the virtual power supply lines stop floating. The voltage across the NMOS or PMOS transistor which is suspended parallel to sleep transistors' output clamps the virtual supply lines. The state of a circuit is maintained by this method and the discharge current in this mode is increased and the transition time gets reduced for the input switching from high to low. When the sleep transistors are switched ON, the current flowing through the circuit become less and hence the dissipation becomes low.

Moreover, the virtual ground potential helps in leakage reduction. Higher value of the virtual ground potential helps in attaining better leakage savings but it upshots in much wake-up time since a lot of charge has to drain through the footer sleep transistor. Hence, a trade-off is essential between leakage savings and wake-up penalty. Moreover, as NMOS sleep transistor gate bias is raised, the voltage in the ground rail reduces and it results in increased leakage power.

Power gating induces switching noises namely the power and ground bounce noises on the power and ground rails. This occurs at the switching of transistors from snooze to active mode. One of the essential circuit noise components is inductive noise. Inductive noise arises due to parasitic inductances from package pins, bonding wires, and on-chip IC interconnects. Voltage fluctuation is generated in case of time domain difference in inductor current. These fluctuations are more on ground and power lines when there is simultaneous switching in the output. Large amount of current flows into the ground lines when the header/footer is activated. Ground bounce can be minimized by decreasing the footer size. Transistors and wires are more due to power gating technique. A more number of transistors are used due to

data retention circuit. In general, the proportion of the amount of data to be maintained across the virtual rails and the outputs to be taken increases wire length and area.

4 Optimal Delay Gates

4.1 Optimal Delay NOT Gate

CMOS inverter has one PMOS transistor and one NMOS transistor. An extra low-threshold PMOS P4 included in circuit improves the output of the inverter and thereby throughput is enhanced. Moreover, a NMOS N3 with high threshold and PMOS P6 with high threshold are connected in parallel to power gating PMOS transistors P2, P3, and P5 in the pull-up network to reduce the delay of the circuit. Furthermore, P7, a high threshold transistor is linked parallel to N2, a high threshold transistor, in the pull-down network. This transistor P7 minimizes the leakage power in the sleep mode. Also, by using reverse body bias circuitry, leakage power in the inactive mode can be further suppressed.

This technique introduces single threshold voltage drop across the sleep transistors. In the static mode, when $\text{sleep}_{\text{pmos}}$ is given logic High and $\text{sleep}_{\text{nmos}}$ is set logic Low, virtual ground rail is clamped to $V_{\text{dd}} + V_{\text{thp}}$, where V_{thp} is the threshold voltages of the PMOS P7 transistor. Voltage across the logic circuit is lessened as the charge retained in the power supply bar is reused to charge the ground rail which is not actual but virtual in the standby mode through the transistor P7. Also, by joining the PMOS substrate and NMOS substrate in the gated circuit to the real supply voltage and real ground line, a novel threshold voltage could be achieved. This new threshold voltage occurs because reverse body bias for the entire transistors in the logic circuit reduces leakage current. In the sleep mode, when low value is applied to the input, P4 would be ON and hence voltage is fed back to the input from the virtual ground and thereby power is decreased in the static mode. However, when high input is applied, P4 would become off and hence the virtual ground voltage might not be able to feed back to the input. Hence, drop in power in the static mode is more only when low input is applied in the input.

In the dynamic mode of operation, $\text{sleep}_{\text{pmos}}$ (P2, P3, and P5) and additional transistors (N3 and P6) are given logic low. In this mode, when the input is low, transistor P4 helps in bringing the leakage current in N1 to the input and thereby active mode power consumption is reduced. When high input is given, leakage in N1 is drained through N2 to the ground and moreover connection to supply voltage is cut off and hence the power consumption is low. Thus, when the low input is applied, high threshold voltage transistor N2 joins NMOS transistor N1 which is ON to the ground.

Active power dissipation and static power dissipation of these inverters are compared in Tables 1 and 2. For the suggested techniques, the transistors' width

Table 1 NOT gate's average power consumption in active mode

Input	CMOS NOT gate (nW)	Optimal delay NOT gate (nW)
0	132.5	56.94
1	132.4	56.94

Table 2 NOT gate's power consumption in static mode

Input	CMOS NOT gate (pW)	Optimal delay NOT gate (pW)
0	22.05	4.17
1	31.54	18.14

Table 3 Transistors and their width utilized in optimal delay NOT gate

Method	Transistors (HVT)	Power gating transistors' width nm	Power gating NMOS transistors' width nm
Optimal delay NOT gate	P2, P3, P5, P6, P7, N2, N3	P2, P3, P5-600 P6, P7-120	120

(HVT) and the list of HVT employed in the circuit are shown in Table 3. In the logic circuits (Fig. 1), low threshold voltage transistors (LVT) are used and all the LVT have the width of 120 nm as width other than those shown in the tables.

4.2 Optimal Delay NAND Gate

The throughput of the NAND gate is enhanced by the adding an extra transistor, a HVT PMOS P7. Here, the PMOS P7, gate, and source are joined together and the input in2 is connected to the transistor P7 gate or drain and the source is linked to the virtual ground and also to the common ground as shown in Fig. 2.

This HVT transistor included in the non-critical path reduces active dynamic power and sleep power consumption to a great extent without affecting the working of the circuit.

Moreover, reverse body bias is applied to reduce standby leakage power. Furthermore, power gating transistors P1, P2, and P5 are connected in the PMOS pull-up setup and N3 is connected in the NMOS pull-down setup to shrink the static power consumption of the circuit. But these sleep transistors upsurge the dynamic active power and circuit delay. Hence, facility is made for the reduction the delay of the circuit by the inclusion of transistors N4 and P6, respectively. Transistors P8 and P9 are having high threshold voltage and are connected in parallel to HVT N3 to decrease standby leakage. The output of CMOS NAND gate has high output when any one of the input goes low. But when the inputs go high in both inputs, then the output goes low.

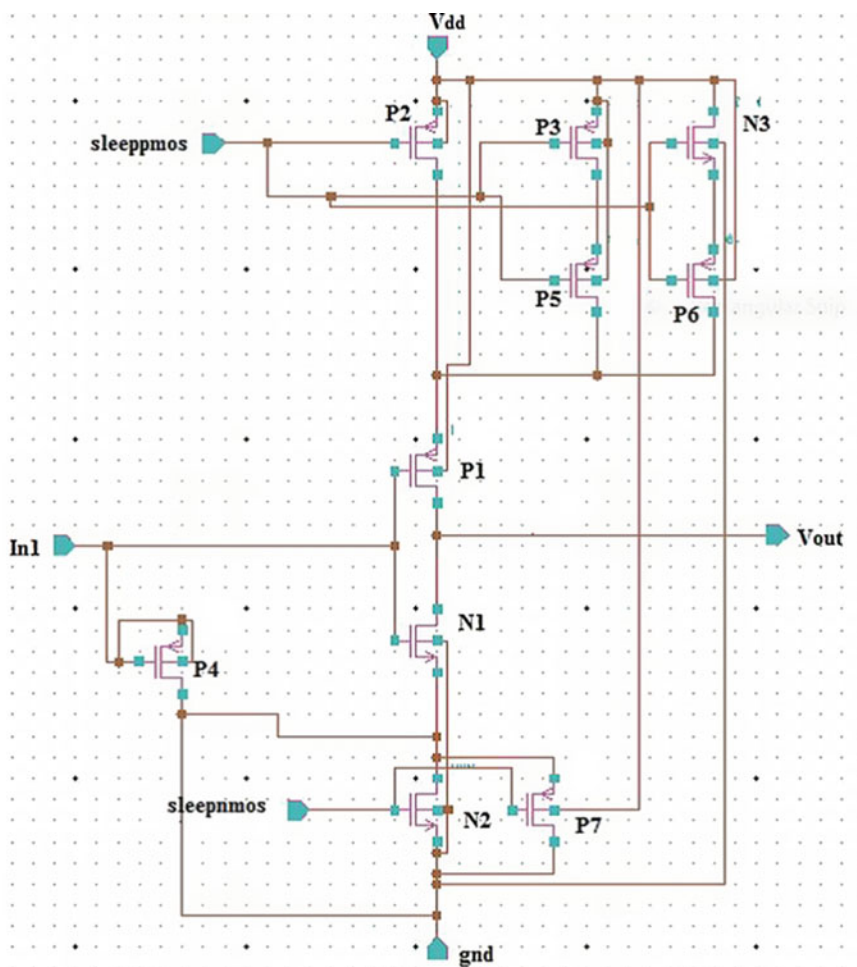


Fig. 1 Optimal delay NOT gate

In the active mode of operation, $\phi_{pmossleep}$ is given low and $\phi_{nmossleep}$ is given high value and HVT PMOS P1, P2, P5, P6 and HVT NMOS N3 are activated. As these transistors, P1, P2, and P5, have low ON resistances, the virtual supply rail almost behaves as the real power supply rail. When the inputs in1 and in2 are made high, the output of the circuit goes low as both the PMOS P3 and P4 are OFF and the transistors N1 and N2 are ON and with the assistance of transistor N3, the current in transistors N1 and N2 drains to the ground and thereby minimizing dynamic power consumption. Likewise when both the inputs are made low, the transistors N1 and N2 in the logic circuit are switched OFF, and the output goes high as the PMOS transistors P3 and P4 are switched ON. Here, the current in the NMOS N3 streams through the transistor P7 as it is switched ON and in this manner active mode power

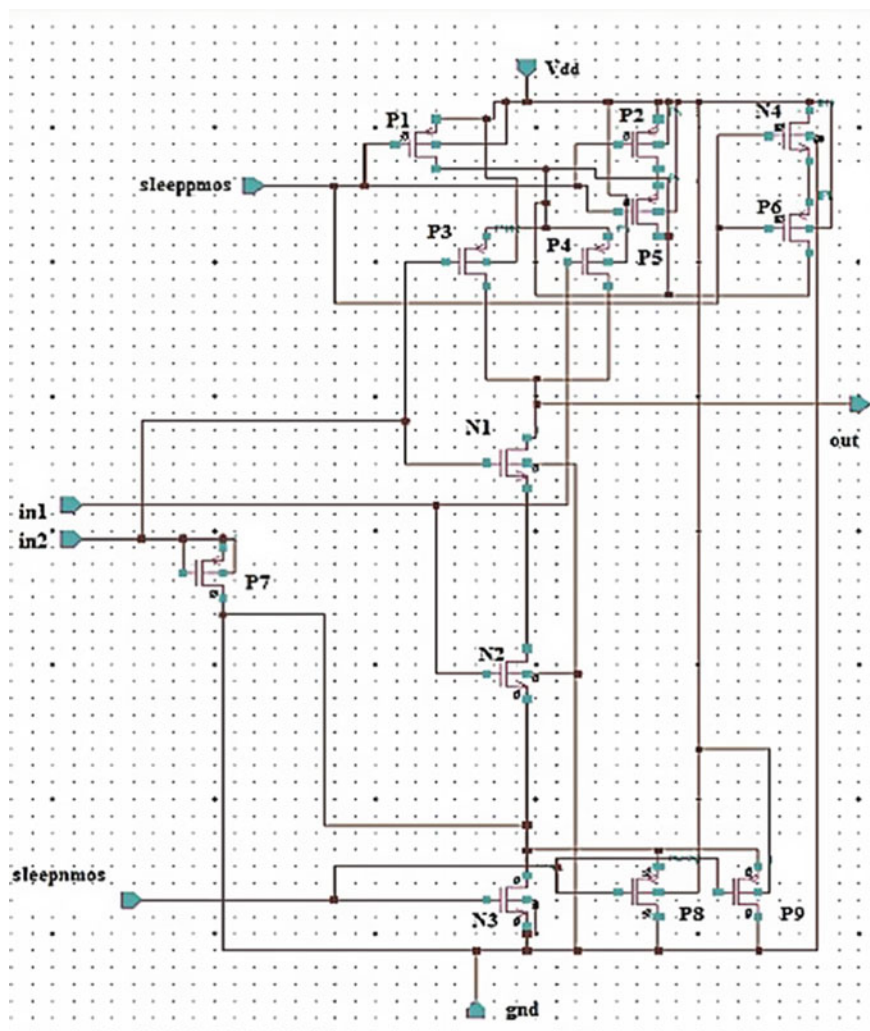


Fig. 2 Optimal delay NAND gate

dissipation is curtailed. When the inputs are made high and low for in1 and in2, respectively, the output is made high as transistor P3 is turned ON and the PMOS P1, P2, P5, and P6 are switched ON. Moreover, the current in the transistor N2 goes to in2 through the transistor P7 and in this manner dynamic power dissipation is minimized. When in1 is made low and in2 is made high, the output is driven high as the PMOS P4 is ON and the NMOS transistor N2 is turned OFF. RBB helps in draining the leakage current in N1.

In case of sleep mode, power gating method reduces the leakage power by using power gating transistors through the input given through pmossleep and nmossleep.

Table 4 NAND gate's average power consumption in active mode

Input	Standard CMOS (nW)	Optimal delay NAND gate (nW)
00	234.40	94.26
01	35.93	24.92
10	31.93	21.80
11	234.70	93.36

Table 5 NAND gate's power consumption in static mode

Input	Standard CMOS (pW)	Optimal delay NAND gate (pW)
00	6.33	6.52
01	21.18	8.52
10	22.05	5.74
11	63.07	2.34

Table 6 Transistors and their width utilized in optimal delay NAND gate

Method	Transistors (HVT)	Power gating transistors' width nm	Power gating NMOS transistors' width nm
Optimal delay NAND gate	P1, P2, P5, P6, P7, P8, P9, N3, N4	P1, P2, P5-960 P6, P7, P8, P9-120	120

In the standby mode, the set up turns off all the sleep transistors. This detaches the NAND gate logic circuit from the supply rail and ground rail. This structure minimizes leakage power to a vast extent and also the circuit's average dynamic power and delay are also minimized but it upturns the area of the circuit.

High threshold voltage NMOS transistors are made smaller in size in comparison to PMOS transistors which have high threshold voltage. This is done as the NMOS transistor ON resistance is less compared to PMOS transistor ON resistance for the similar width. Also, it should be noted that dynamic power consumption can be decreased by increasing the input rise time and fall time and the delay is increased and vice versa.

Active power dissipation and static power dissipation of these NAND gates are compared in Tables 4 and 5. For the suggested techniques, the transistors' width (HVT) and the list of HVT employed in the circuit are shown in Table 6.

4.3 Optimal Delay NOR Gate

Here, two additional transistors N1 and N2 used are high-threshold NMOS transistors and their connection is shown in Fig. 3. Both transistors' source terminals are tied together to V_{GND} and another PMOS transistor P7, which is also a HVT transistor,

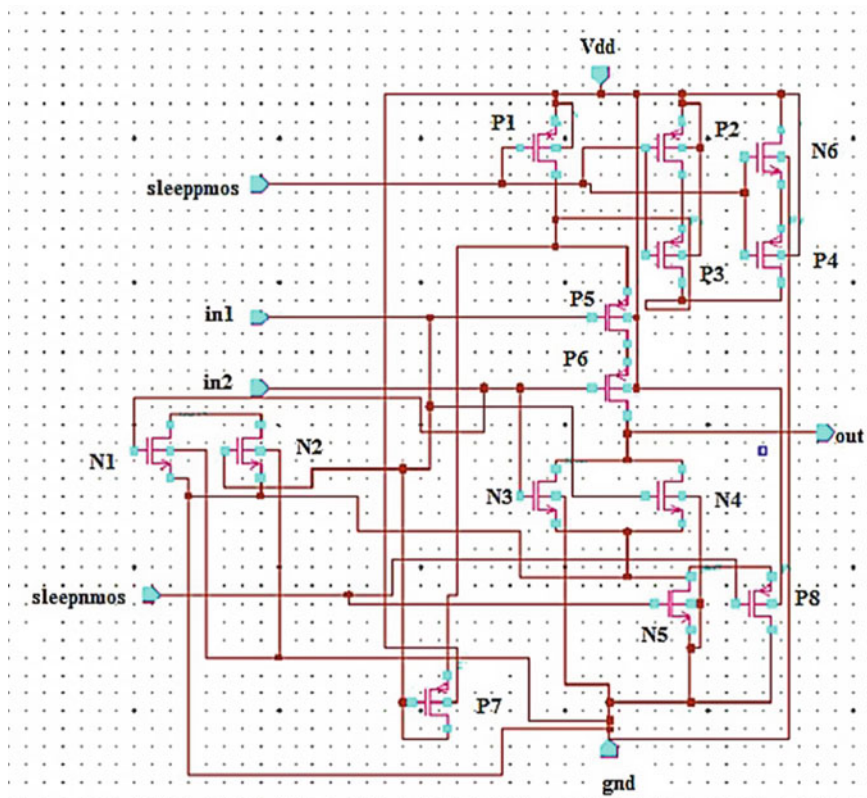


Fig. 3 Optimal delay NOR gate

with its drain and gate terminal shorted and the source of P7 is joined to virtual supply V_{DD} . Moreover, HVT P4 and N6 are connected in parallel to power gating transistors and HVT P8 is connected in parallel to power gating transistor N5. In general, NOR gate output is low if at least one input is made high and the NOR gate output is high if both the inputs are made low.

In the active mode, when in1 and in2 are made high, these two transistors N1 and N2 which are high threshold voltage transistors are ON and the transistors in the logic circuit are switched ON. Hence, the output goes low because of the pull-down transistors N3 and N4 and also the transistors P5 and P6 are turned off. When in1 is low, the PMOS transistor P5 is turned ON and the input in1 is fed to transistor P7. This switches ON the PMOS transistor P7 whose source is joined to virtual power supply, V_{DD} and this helps in pulling the output high. If in2 is made high, then transistors P6 is OFF and this pulls the output low. Further, if the next input is also made low, P6 is switched ON and the NMOS transistors in the circuit are turned OFF and this results in high output. When the inputs are high and low for in1 and in2, respectively, the transistor P5 is OFF, and the transistor P6 is switched ON and the

Table 7 NOR gate’s average power consumption in active mode

Input	Standard CMOS (nw)	Optimal delay NOR gate (nw)
00	210.60	230.2
01	52.95	177.4
10	59.63	182.4
11	210.60	231.7

transistor P7 is turned OFF and the output goes Low though the PMOS transistor P6 is ON. This happens as the PMOS transistor P5 is OFF. This technique achieves in decreasing the leakage current of the circuit. In the sleep mode of operation, when the inputs are high and low for in1 and in2, respectively, the transistor P5 is switched OFF and the output is not attached to the supply line. When in1 is made high and also in2 is made high, the PMOS transistors P5 and P6 are switched OFF and hence the output is no longer connected to power supply rail. Hence, in both these cases, static power dissipation is significantly reduced. However, in the other two conditions also, very little leakage current flows through the circuit as the PMOS transistor P8 is switched OFF and thereby static power dissipation is minimized to an extent.

Besides, the threshold voltage of the transistors is raised in the static mode using the technique reverse body bias. This reverse body biasing is achieved by joining the PMOS substrate to the power supply rail and this increases *N*-well voltages of the PMOS transistors. Hence, the PMOS transistors’ threshold voltage is raised which afterwards helps in the lessening of leakage current in PMOS transistors. Similarly, in case of NMOS transistors, the NMOS transistors’ body is connected to the ground rail which in turn decreases the *P*-well voltages of the NMOS transistor, which helps in raising the NMOS threshold and thereby leakage reduction happens in the NMOS transistors. But in order to achieve a slight rise in threshold voltage, a large supply voltage is needed. Hence this method is not so effective, when the power supply voltage is decreased.

Active power dissipation and Static power dissipation of these NOR gates are compared in Tables 7 and 8. For the suggested techniques, the transistors’ width (HVT) and the list of HVT employed in the circuit are shown in Table 9.

Table 8 NOR gate’s power consumption in static mode

Input	Standard CMOS (pW)	Optimal delay NOR gate (pW)
00	44.11	4.12
01	31.54	3.20
10	30.63	1.03
11	10.69	0.95

Table 9 Transistors and their width utilized in optimal delay NOR gate

Method	Transistors (HVT)	Power gating transistors' width nm	Power gating NMOS transistors' width nm
Optimal delay NOR gate	P1, P2, P3, P4, P7, P8, N1, N2, N5, N6	P1, P2, P3-600 P4, P7, P8-120	120

5 Simulation Results

The novel technique was implemented in a full adder circuit in order to decrease the static and dynamic power within 45 nm CMOS technology and the supply voltage used is 0.6 V. CADENCE design platform is used for the design and simulation of the circuit. All circuits are simulated in the active and sleep mode and the power dissipation is observed. In the static mode, PMOS transistors which are used for power gating are kept at 0.6 V and NMOS transistors in the footer are kept at ground potential or 0 V. In the dynamic mode, power gating transistors in the header section are connected to ground and NMOS transistors in the footer section are applied a pulse varying from 0 to 0.6 V. The pulse width and period are kept as 700 ps and 1.4 ns, respectively. The fall and rise time of the inputs are kept within 45 ns, 52 ns and 55 ns for NOT gate, NOR gate and NOR gate, respectively.

CADENCE result browser and calculator is implemented for measuring the static and average power consumption for all operating conditions. Tables 1 and 2 shows the static power dissipation and dynamic power dissipation of the optimal delay NOT gate and compared the simulated results with standard NOT gate. Likewise Tables 4 and 5 show the static and dynamic power consumption of NAND gate. NOR gate results are listed for all possible inputs and compared with standard NOR gate in Tables 7 and 8. Compared to standard NOT gate, optimal delay NOT gate has less total average dynamic power consumption. Moreover for static power consumption, novel technique is better compared to CMOS technique.

Novel technique of NOT gate has more delay in comparison to CMOS NOT gate as the number of transistors involved in the novel technique is more. The output of optimal delay NOT gate is depicted in Fig. 4.

Tables 4 and 5 tabulates the active and static power dissipation of CMOS NAND gate and optimal delay NAND gate. When compared within these techniques, optimal delay NAND gate consumes a reduced amount of static power and dynamic power. Table 11 brings out that delay in case of novel NAND gate is high. The simulated result of proposed NAND gate is given in Fig. 5.

The average power consumption and static power consumption of CMOS NAND gate and optimal delay NAND gate are listed in Tables 4 and 5, respectively. Compared to standard CMOS NAND, novel method dissipates a lesser amount of static power dissipation and average dynamic power dissipation. However novel method has more delay as shown in Table 11. The simulation waveform of optimized delay NAND gate is depicted in Fig. 5.

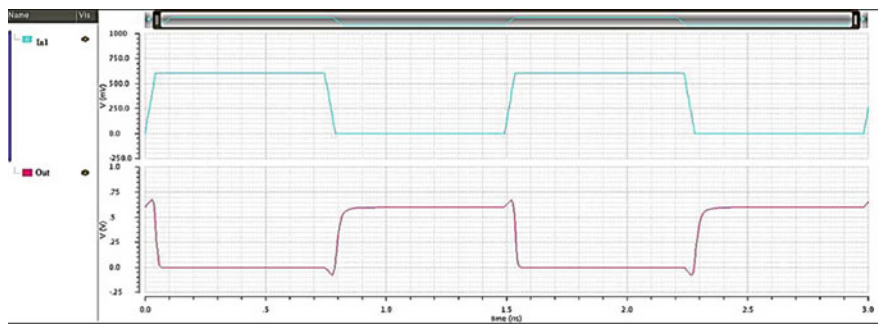


Fig. 4 Optimal delay NOT gate simulated result in 45 nm CMOS

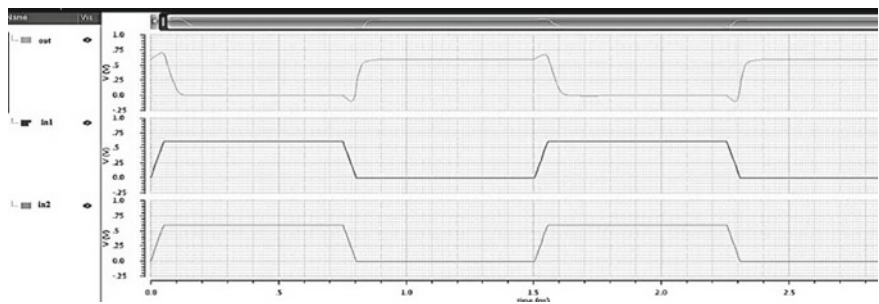


Fig. 5 Optimal delay NAND gate simulated result in 45 nm CMOS

Table 10 Delay of standard NOT gate and proposed NOT gate

Input	Standard CMOS (ps)	Optimal delay NOT gate (ps)
0	12.69	28.34
1	12.66	28.36

Table 11 Delay of standard NAND gate and proposed NAND gate

Input data pattern	Standard CMOS (ps)	Optimal delay NAND gate (ps)
In1 = In2 = 0 → 1	34.13	45.80
In1 = 1, In2 = 0 → 1	29.26	42.69
In1 = 0 → 1, In2 = 1	30.90	53.76
In1 = In2 = 1 → 0	33.73	43.49
In1 = 1, In2 = 1 → 0	29.35	42.72
In1 = 1 → 0, In2 = 1	30.58	52.26

Table 12 Delay of standard NOR gate and proposed NOR gate

Input data pattern	Standard CMOS (ps)	Optimal delay NOR gate (ps)
In1 = In2 = 0 → 1	19.99	46.07
In1 = 0, In2 = 0 → 1	20.31	45.87
In1 = 0 → 1, In2 = 0	23.25	60.13
In1 = In2 = 1 → 0	21.04	53.08
In1 = 0, In2 = 1 → 0	20.87	45.96
In1 = 1 → 0, In2 = 0	23.78	60.70

Tables 7 and 8 shows the total average active and standby power consumption of standard NOR gate and optimal delay NOR gate. Here, optimal delay NOR gate consumes more average power in comparison with the CMOS NOR as the number of transistors are involved are more. However, when static power is compared with CMOS NOR gate, power consumption is lesser in case of optimal delay NOR gate. Delay is more in optimal delay NOR gate as extra NMOS and PMOS transistors are added and it is shown in Table 12. The simulated waveform of proposed NOR gate is shown in Fig. 6.

A full adder circuit is employed to exhibit the advantages of novel gates. This full adder is built with standard NAND gates and the same is simulated with 700 ps pulse width and 1.4 ns period. A single bit adder cell works well but for practical applications, it might not produce appropriate results. When a large number of single bit full adders are connected in series, the successive cells might not be capable to offer suitable input signal to the next adder cells which are to be driven. This causes cumulative decline in the signal value which will lead to errors in the output and the malfunctioning of the circuit happens when operated using different low voltages. To indicate the performance and the capability to drive in cascaded form, a 32 bit ripple

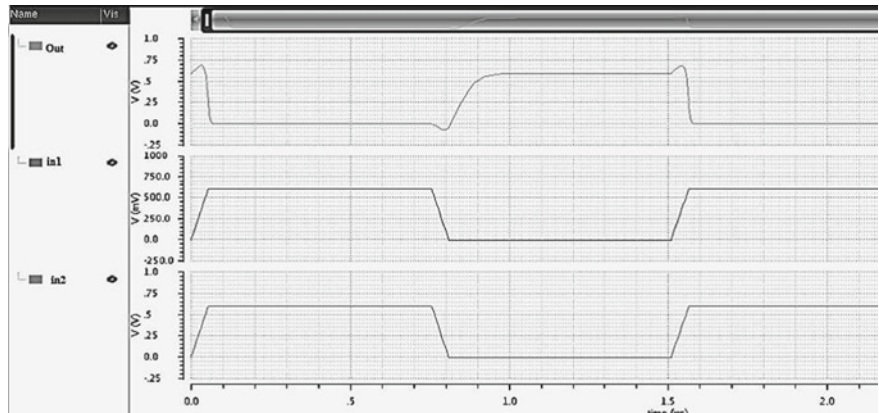


Fig. 6 Optimal delay NOR gate simulated result in 45 nm CMOS

Table 13 Comparison of average power dissipation of different full adders in 45 nm technology at 670 MHz and 0.6 V V_{DD}

Techniques	Single bit (μ W)	4 bits (μ W)	8 bits (μ W)	16 bits (μ W)	32 bits (μ W)	Maximum operating frequency (MHz)	Remarks
CMOS	1.18	5.87	11.88	23.9	47.9	670	–
TGA* [15]	1.28	4.44	8.76	17.17	33.50	100	Unstable output
10T* [16]	0.31	1.04	2.35	5.01	10.31	0.5	Unstable output
Hybrid CMOS* [17]	2.07	13.12	29.89	63.68	128.10	500	Unstable output
ULPFA* [18]	1.08	2.73	5.72	11.86	24.13	100	Unstable output
High speed* Hybrid [19]	1.23	4.64	9.30	18.43	37.01	200	Unstable output
Optimal delay NAND gate	0.67	2.96	6.22	12.54	25.85	670	–

carry adder with $V_{DD} = 0.6$ V is used to simulate all the various techniques depicted in Table 13 and a comparison is done with the proposed technique and the other prevailing full adders quoted in [15–19] to show its usage in practical applications and their outputs are charted in Tables 13 and 14. In order to compare all these techniques, two inputs are given values from 0 to 0.6 V and last input is assigned as 0.6 V–0. The novel technique is simulated for different input values and their output is depicted in Fig. 7 with $V_{DD} = 0.6$ V.

In Table 13, the adders marked with asterisks in the tabulation have unstable outputs for $V_{DD} = 0.6$ V and 670 MHz operating frequency and cannot be used for real-time setup. We have constructed the basic adder only with NAND gates since the regular adder with 28 transistors could not have 0.6 V for proper operation. From the table, it could be inferred that average power and static power dissipation of TGA is less and also it produces degraded output for higher bits. Hence, TGA might be recommended for only single bit. Also, it is noted that the TGA output never touches zero when the expected output is low. Among all the techniques which have proper outputs in Table 13, optimal delay NAND gate technique shows less dynamic power dissipation. High-speed hybrid technique and hybrid CMOS technique have very much higher static power consumption and can be used in VLSI applications where static power consumption is not a major issue.

However, static power in case of optimal delay NAND gate technique is less when it is compared with various other methods. Hence, this novel one can be used in practical applications where ever required needed.

Table 14 Comparison of static power dissipation of different full adders in 45 nm technology at 670 MHz frequency and 0.6 V V_{DD}

Techniques	Input	Single bit (nW)	4-bit (nW)	8-bit (nW)	16-bit (nW)	32-bit (nW)
CMOS	000	0.29	1.16	2.31	4.63	9.26
	111	0.32	1.27	2.54	5.09	10.18
TGA [15]	000	12.42	49.45	98.81	197.55	395.02
	111	9.28	37.07	98.70	148.24	296.48
10T [16]	000	7.09	28.01	55.92	111.72	223.33
	111	0.003	0.02	0.06	0.13	0.27
Hybrid CMOS [17]	000	34.29	136.49	274.07	548.10	1096.18
	111	31.86	126.90	253.63	507.09	1014.00
ULPFA [18]	000	4.31	22.62	45.47	90.49	180.99
	111	3.66	6.93	13.85	27.71	55.41
High-speed hybrid [19]	000	14.27	57.00	114.11	228.20	456.45
	111	15.92	63.65	127.29	254.58	509.14
Optimal delay NAND gate	000	0.05	0.19	0.37	0.75	1.49
	111	0.05	0.20	0.39	0.78	1.56

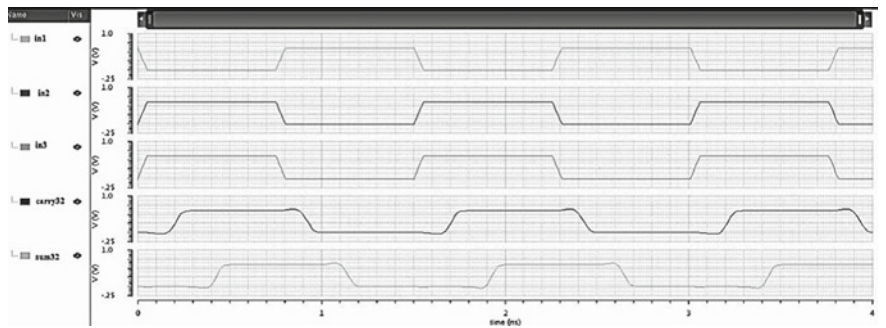


Fig. 7 Proposed technique 32-bit RCA output waveform in 45 nm CMOS

Table 15 brings out the comparison of the delay and the power delay product for various methods. 10T transistor technique and ULPFA could be operated only at low frequency. Among all the techniques shown in Table 15, high-speed hybrid has very less power delay (PDP) up to 8 bits compared to all the other techniques. However, high-speed hybrid technique and hybrid CMOS might not be used when there is any change in the input switching pattern and could be used only where there is no need to consider static power dissipation. Moreover, the output of high-speed hybrid adder circuit could not touch zero when there should be a low output. In other words, this high-speed hybrid has a weak zero.

Power delay product of optimal delay NAND gate technique is more favorable than that of CMOS technique confirming its superiority in design. Moreover, in optimal

Table 15 Comparing delay and power delay product of full adders in 45 nm technology at 0.6 V V_{DD}

Techniques	Single bit		Eight bit		Sixteen bit		32 bit	
	Delay	PDPP	Delay	PDP	Delay	PDP	Delay	PDP
CMOS	92.38	0.11	0.294	3.50	0.294	7.03	0.294	14.08
TGA [15]	186.85	0.24	*	—	*	—	*	—
10T [16]	**	—	**	—	**	—	**	—
Hybrid CMOS [17]	101.26	0.21	***	—	***	—	***	—
ULPFA [18]	***	—	***	—	***	—	***	—
High-speed hybrid [19]	374.35	0.46	0.001	0.01	*	—	*	—
Optimal delay NAND gate	128.00	0.09	0.387	2.41	0.387	4.85	0.387	10.0

*Denotes degraded output, **denotes unstable output, ***denotes functionality affected

delay NAND gate technique, the static power is very much less in comparison to all the other listed techniques. Active mode power consumption is also minimized in this novel technique and we get full output voltage swing.

6 Conclusion

The paper proposes optimal delay techniques of NOT, NAND, and NOR gates and the analysis of 32-bit RCA is done using these novel gates. The proposed technique using optimal delay NAND gate performs excellently with supply voltage reduction and has better noise immunity as compared to the static CMOS adders. This performance analysis was accomplished in 45 nm technology for 32-bit ripple carry adder. The novel method is correlated with few available techniques for 32-bit RCA. The simulated software result exhibits a colossal drop in case of static power dissipation for proposed method implemented for 32-bit RCA. Compared to static CMOS adder, novel technique has 46% dynamic power reduction and has 84.3% static power reduction and 28.98% PDP reduction. This technique is mainly promising for circuits that operate for a long time in the standby mode. Future work includes implementation of the proposed technique with better reduction in dynamic power for highly efficient circuits.

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