

An In-Band Full-Duplex Low Noise Amplifier Integrated With an Electrical Balance Duplexer Without Explicit Matching

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Abstract—This letter presents a low noise amplifier (LNA) integrated with an electrical-balance duplexer (EBD) for in-band full duplex operation in a 65-nm bulk CMOS process. A simultaneous noise and input matching (SNIM) structure consisting of a large transistor and hybrid transformer for EBD is proposed. The proposed structure does not require an additional matching circuit between the LNA and the antenna (ANT). Furthermore, the use of a large transistor in the SNIM helps minimize the noise figure (NF). The core size of this LNA is $0.86 \times 0.33 \text{ mm}^2$. The measurement results show 14.6–16.5 dB ANT-RX (receiver) gain, 4.29–4.53 dB TX-ANT loss, 30.6–34.5 dB isolation, and 5.33–5.37 dB NF. The LNA has an input 1-dB compression point (IP1dB) of -18.1 dBm at 15 GHz and the power consumption is 22 mW.

Index Terms—CMOS, electrical-balance duplexer (EBD), in-band full-duplex (IBFD), Ku-band, low noise amplifier (LNA).

I. INTRODUCTION

KU-BAND has been used for radar and satellite communication, and the potential for use in the frequency band for LEO satellite networks for 6G has been recently discussed [1], [2]. The 6G requires a high-frequency spectrum efficiency similar to 5G, which can be improved through full-duplex communication. The critical challenge in an IBFD system is the cancellation of transmitter (TX) self-interference (SI). The use of multiple antennas (ANTs), circulators, electrical balance duplexer (EBD), etc., [3], [4], [5], [6], [7], [8] has been suggested to suppress or remove SI. Because the circulator cannot be integrated into IC with a transceiver, and the technique of multiantenna requires more than two ANT per channel transceiver, they are not suitable for the Ku-band full-duplex system wherein an array system is used to overcome path loss. On the other hand, the EBD can implement fully integrated IBFD with the transceiver, and it requires only one ANT per channel. The most widely adopted EBD is the hybrid transformer with a symmetrical tapping structure, which has a theoretical insertion loss of 3 dB in both the TX and receiver (RX) paths. As shown in Fig. 1(a), a typical EBD uses an additional matching network between EBD and RX or TX channels, resulting in additional loss in

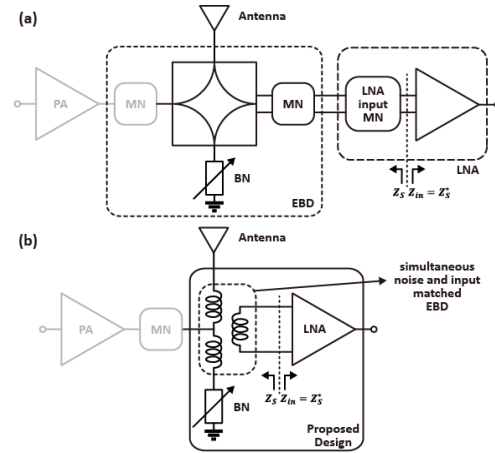


Fig. 1. Block diagram of full duplexers. (a) Conventional EBD with additional matching networks. (b) Proposed simultaneous noise and input matched EBD and LNA.

the TX and RX paths. These losses represent a bottleneck in the design of high-performance IBFD systems using EBD.

In this study, we propose a low noise amplifier (LNA) integrated with EBD as shown in Fig. 1(b). The proposed LNA improves the noise characteristics by applying the simultaneous noise and input matching (SNIM) technique using the large transistor and removing additional input matching network using combined EBD and LNA.

II. PROPOSED IBFD LNA DESIGN

Fig. 2 shows a schematic of the proposed LNA. Before integrating EBD and LNA, the structure of LNA should be selected among single-ended and differential structures. Although both structures can be integrated with EBD, the linearity of the differential structure can be greater than that of the single-ended structure by 3 dB, and thus, the proposed LNA circuit is composed of a differential structure. In general, the balun used in the CMOS LNA is a transmission line transformer (TLT), and the impedance mismatch occurs structurally. Because the impedance mismatch of the differential pair results in isolation degradation, a cascode structure with excellent input–output isolation is used in the second stage. For the same reason, the interstage matching network is configured according to the same matching network pair in order to prevent impedance mismatch.

The EBD used in this study is a hybrid transformer as shown in Fig. 3(a), and it must satisfy the following [9]:

$$Z_{\text{ANT}} = Z_{\text{BAL}} \quad (1)$$

$$Z_{\text{TX}} = Z_{\text{ANT}}/2. \quad (2)$$

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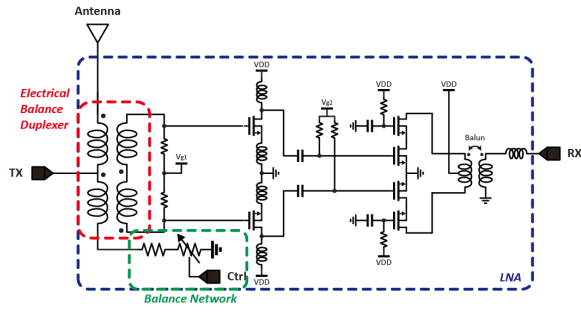


Fig. 2. Schematic of LNA with merged duplexer.

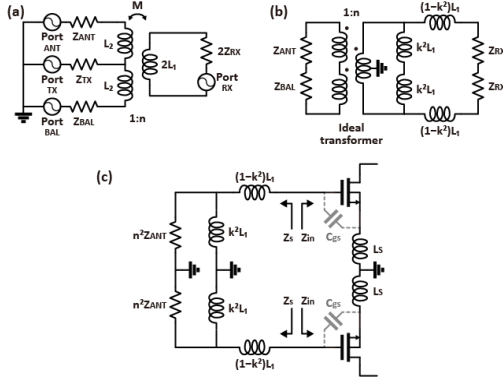


Fig. 3. Schematics of (a) hybrid transformers as in-band full-duplexer, (b) its equivalent circuit as an impedance transformer, and (c) equivalent circuit of differential pair.

In the RX port in Fig. 3, the TX port appears to be an open circuit. Therefore, a hybrid transformer can be interpreted as a transformer with a primary coil of $2L_1$, secondary coil of $2L_2$, and a mutual inductance M . At this time, the coupling coefficient k and the turn ratio n of the transformer can be expressed as follows. An equivalent circuit as shown in Fig. 3(b) can be created [8], [10], [11]

$$k = \frac{M}{2\sqrt{L_1 L_2}} \quad (3)$$

$$n = k\sqrt{\frac{L_1}{L_2}}. \quad (4)$$

The differential pair of LNA proposed using (4) and Fig. 2(b) can be expressed as shown in Fig. 3(c). The equivalent circuit in Fig. 2(c) is similar to the structure of the SNIM network wherein large transistors are used [12], [13]. The use of a large transistor in the SNIM technique helps improve noise figure (NF) because the series inductance in Fig. 3(c) is reduced, as shown in Fig. 3(c). The source impedance Z_S and input impedance Z_{in} of the proposed LNA are as follows:

$$Z_S(j\omega) = (n^2 Z_{ANT} || k^2(j\omega L_1)) + (1 - k^2)(j\omega L_1) \quad (5)$$

$$Z_{in}(j\omega) = j\omega L_S + \frac{1}{j\omega C_{gs}} + \frac{g_m L_S}{C_{gs}}. \quad (6)$$

For SNIM, the optimum noise impedance (Z_{opt}), Z_S , and Z_{in}^* must satisfy by the following equation:

$$Z_{in}^* = Z_{opt} = Z_S. \quad (7)$$

From (3)–(7), n and L_2 are arranged, as shown in the following equations:

$$n^2 = X \left(\frac{R_S}{(\omega L_2)^2} + \frac{1}{R_S} \right) \quad (8)$$

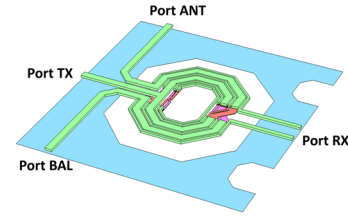


Fig. 4. 3-D structure of the EBD.

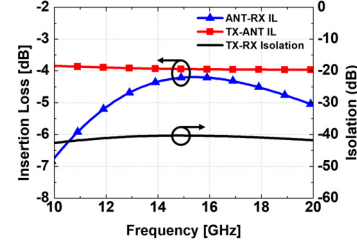


Fig. 5. S-parameter simulation results of in-band full-duplexer using hybrid transformer.

$$L_2 = \frac{R_S}{\omega} \frac{Y - \sqrt{Y^2 - \frac{4X^2}{k^2} \left(\frac{1}{k^2} - 1 \right)}}{2X \left(\frac{1}{k^2} - 1 \right)} \quad (9)$$

$$X = \frac{g_m L_S}{C_{gs}}, \quad Y = \frac{1}{\omega C_{gs}} - \omega L_S$$

$$Y^2 - \frac{4X^2}{k^2} \left(\frac{1}{k^2} - 1 \right) > 0 \quad (10)$$

where g_m , C_{gs} , and L_S are determined so that Z_{opt} is equal to Z_{in}^* . Because L_2 is a real value, (9) must satisfy (10). At this time, because g_m , C_{gs} , and L_S have been determined, the usable range of k can be found through (10). The typical values for k for monolithic transformers are in the range 0.6–0.9. Because C_{gs} of the proposed LNA is large, the value of k , which satisfies (10) becomes large. As k increases, the NF decreases due to a small series inductor $(1 - k^2)L_1$. Therefore, a large k should be used to lower NF. However, it is difficult to design a hybrid transformer with a large k . Therefore, the k of the hybrid transformer was selected as 0.9, which is a general size of k and a value that satisfies (10). According to the determined k , (4), (8), (9), the n and L_1 of the hybrid transformer are approximately 1.57 and 2.0 nH, respectively. Fig. 4 shows the 3-D structure of the EBD used in the proposed LNA. The values of k , n , and L_1 were changed to approximately 0.85, 1.57, and 2.6 nH, according to parasitic components, respectively. The electromagnetic (EM) simulation results of EBD are shown in Fig. 5. A 4.21 dB loss in the path from the ANT to the RX, 3.95 dB loss in the path from the TX to the ANT, and 40.34 dB isolation in the path from the TX to the RX are observed at 15 GHz.

The SNIM mechanism of LNA is shown in Fig. 6. First, the source inductance L_S and the size of the transistor were chosen such that Z_{opt} equals Z_{in}^* . For the size of the transistor, the largest value satisfying (10) was used. Second, the small series inductance $(1 - k^2)L_1$ shifts Z_{in}^* and Z_{opt} to a constant admittance circle. Third, the shunt inductance $k^2 L_1$ moves Z_{in}^* and Z_{opt} to the real axis, where the imaginary part is zero. Finally, the ideal transformer moves Z_{in}^* and Z_{opt} from $n^2 Z_{ANT}$ to Z_{ANT} .

III. MEASUREMENT RESULTS

Fig. 7 shows a microphotograph of the fabricated LNA. The core area of the circuit is $0.86 \times 0.33 \text{ mm}^2$, and the chip

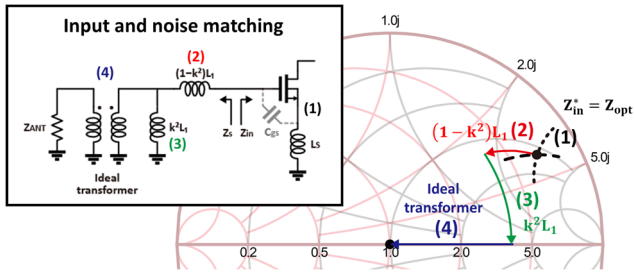


Fig. 6. Noise and input matching mechanism of first stage with merged EBD.

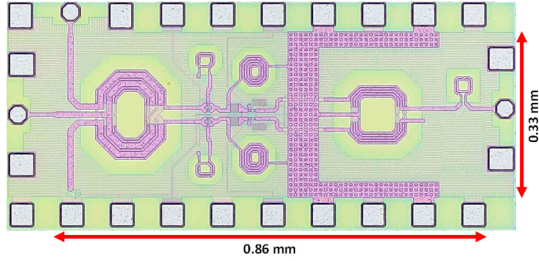
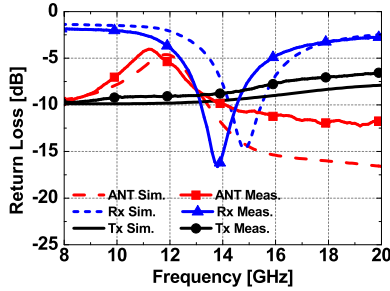
Fig. 7. Fabricated chip microphotograph (core area: $0.86 \times 0.33 \text{ mm}^2$).

Fig. 8. Measured return loss.

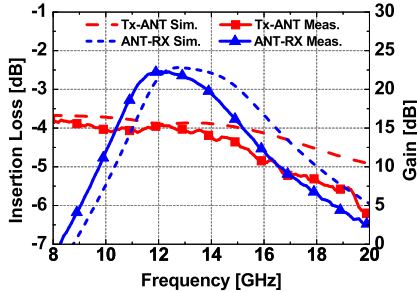


Fig. 9. Measured TX-ANT path insertion loss and ANT-RX path gain.

area including the test pad is $1.01 \times 1.05 \text{ mm}^2$. At a supply voltage of 1.0 V, the power consumption was 22 mW. For the S -parameter measurement, we used a Keysight N5224A network analyzer. Fig. 8 shows the measurement results for the ANT, RX, and TX port return losses. Fig. 9 shows the measurement results for the ANT-RX path gain and TX-ANT path loss. The measured ANT-RX path gain was measured to be 15.79 dB at 15 GHz. The TX-ANT path loss was measured to be 4.38 dB at 15 GHz. Fig. 10(a) shows the measured isolation between the TX input and LNA output ports. An isolation of 34.5 dB at 15 GHz and at least 30.3 dB isolation from 8 to 20 GHz are obtained. Fig. 10(b) shows the simulated NFs and those measured. The average NF is 5.35 dB at 14.8–15.3 GHz. The measured input 1 dB compression point (IP1dB) is -18.1 dBm at 15 GHz, ANT port, as shown in

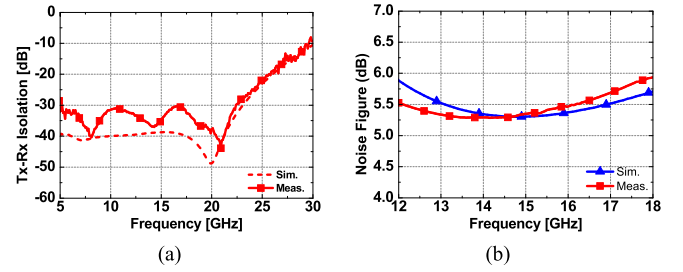


Fig. 10. (a) Measured TX-RX path isolation. (b) Simulated and Measured NF.

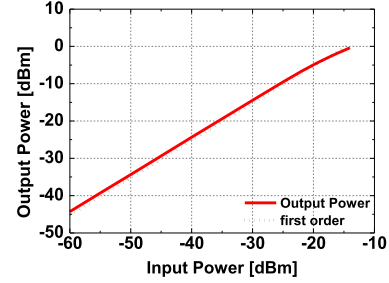


Fig. 11. Measured P1dB.

TABLE I
PERFORMANCE COMPARISON WITH STATE OF THE ARTS

Ref.	JSSC'18[14]	MWCL'18[7]	TNTT'21[16]	This work
Technology	0.18- μm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
Circuit type	EBD+LNA	EBD+LNA +Notch Filter	EBD+LNA	EBD+LNA
Frequency (GHz)	0.7-1.0	1.6-2.2	0.7-1.0 1.8-2.2	14.8-15.3
TX-ANT IL (dB)	3.7-3.9	3.6-3.95	3.5-3.8 3.5-3.9	4.29-4.53
ANT-RX Gain (dB)	4.8-5.5	21.1-24.8	8.7-9.4 3.7-5.9	14.6-16.5
Isolation (dB)	> 40	> 50	> 58.6 > 54.7	30.6-34.5
Noise Figure (dB)	8.7-9.2	6.4-6.8	10.4 12.1	5.33-5.37
ANT to RX P1dB (dBm)				-18.1 at 15 GHz
ANT to RX IIP3 (dBm)	6.4	-12.5	10.4 12.5	
Active area (mm^2)	9.62	1.19	2	0.284
P_{dc} (mW)	48.7-62.5	9.6	28.6	22

Fig. 11. A comparison of these results with those of recently reported full-duplex RX is presented in Table I. The proposed LNA has the lowest NF and smallest active area compared to other full-duplex RXs.

IV. CONCLUSION

In this study, a low-noise amplifier integrated with an electrically balanced duplexer was designed and implemented for an in-band full-duplex system. The proposed LNA combines EBD and LNA to remove unnecessary matching networks, and it improves the noise characteristics by applying the SNIM technique using a large transistor.

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