



On the design and analysis of ultra low-input current sensing trans-impedance amplifier

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Abstract. In this paper, a Trans-Impedance Amplifier (TIA) for ultra-low input current sensing in near-infrared spectroscopy (NIRS) wearable healthcare devices is presented. The proposed TIA consists of two stages to achieve a maximum transimpedance gain (TIG) of 239.86 dB Ω . The -3 dB bandwidth was 10 MHz and the Unity Gain Bandwidth (UGB) was 100 MHz. This TIA can sense and amplify ultra-low-input current in the range of 1 pA to 10 pA, and is used for wearable healthcare devices such as non-invasive glucometers and pulse oximeters. A novel variable trans-impedance gain control circuit and a saturation mitigation circuit were implemented. The input referred noise is 12.9 fA/ $\sqrt{\text{Hz}}$ and the figure of Merit (FoM) is 2078. This TIA consumes 115.31 μW of power at 27 °C from a 1V supply voltage. The proposed circuit was implemented using a Generic Process Design Kit (GPDKit) 45 nm CMOS process. The layout occupied an area of 2264 $\mu\text{m} \times 2191 \mu\text{m}$.

Keywords. Bio-Medical application; High gain; High sensitivity; Infra-Red; Ultra-Low input current; Low power; Near Infra-Red Spectroscopy (NIRS); Non-invasive glucometers; Pulse oximeters; Trans-Impedance gain (TIG); Wearable healthcare devices.

1. Introduction

Biomedical sensors produce extremely weak signals. High-Gain Trans-Impedance Amplifiers are required to amplify the very weak signal in the pico-ampere range into a strong signal before being processed by the Analog-to-Digital Converter and further processed by the microcontroller, Digital Signal Processor (DSP), or computer. A low-current measurement system (LCMS) is necessary for the study and application of medical treatments. Tens of picoamperes can be the lowest current level within a 1–10 kHz bandwidth when using an electrode capacitance of 50 pF [1, 2]. A quick DNA sequencing system is another application of the current measurement techniques. A pair of electrodes passing through a nanopore is used to detect a 10 pA–100 pA current with a 60pF capacitance and a bandwidth of 10KHz [3]. A high-BW optical receiver that can quantify the difference in phase between the reflected and transmitted signals is a crucial characteristic FD for-NIRS employed in biological applications such as intracardiac echocardiography (ICE) [4]. Design [5] offers a large gain bandwidth product (GBW) by trading off high input-referred noise and high power consumption. A TIA design must have several fundamental characteristics, including a

large gain, better linearity, and minimal noise with sufficient bandwidth to amplify a variety of biomedical signals. By achieving a very low input impedance, the TIA can reduce the effects of the photodiode parasitic capacitance, which can limit the bandwidth [6]. The primary -block in biomedical processing systems transforms a sensor current with an amplitude appropriate for subsequent processing from the range of nanoamperes and picoamperes into a proportional voltage. This is accomplished using the current-mode amplifier and shunt feedback mode amplifier topologies. A shunt feedback amplifier uses a current-mode operation to combine the advantages of both current schemes [7].

Compact ultrasound probes use low-noise trans-impedance amplifiers (TIAs), which offer constant variable strength to offset the time-dependent attenuation of the received echo signal [8]. To provide an analog conditioning circuit for wearable, portable, and implantable sensors in biomedical applications, a transimpedance amplifier (TIA) was implemented [9, 10]. For biological applications that are implanted, wearable, or portable, a CMOS fully integrated optoelectronic sensing circuit composed of a Si photodiode and a trans-impedance amplifier has been specially designed and manufactured [11–13]. Low-current sensing circuits for various biomedical applications have been designed and implemented to detect a low input

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current in the range of 50pA-100 pA [14–16]. Adjustable High-Gain Ultra-Low Noise Transimpedance Amplifiers are used in biomedical devices to amplify high-noise-sensitive signals [17–20]. Low-input current signals from biosensors can be detected using a low-noise, high-gain current signal detector based on a resistive feedback trans-impedance amplifier (TIA) [21, 22]. Non-invasive glucometers have been implemented and discussed [23, 24]. Various saturation-mitigation techniques were presented in the section 2.

A conventional telescopic cascode amplifier has a differential pair and cascode pair on top of the differential pair and stacked current mirrors. The current mirrors are biased in saturation owing to the external bias voltages. It has a differential output and requires a complex common-mode back (CMFB) circuit to maintain a fixed common-mode voltage. The open-loop gain of the conventional telescopic cascode amplifier is 30-40 dB. The modified single-ended telescopic cascode amplifier proposed in this study has a modified differential pair with one of the inputs grounded and a cascode pair with an external bias voltage to bias the cascode pair into saturation. The stacked current mirrors are modified to provide a high output impedance to the proposed telescopic cascode amplifier. The proposed current mirrors are self-biased. The open-loop gain of the proposed telescopic cascode amplifier is 59.86 dB Ω . The output impedance provided by the proposed current mirrors can be varied to achieve the required output impedance by varying the bias current of the simple current mirror in parallel. By changing the bias current, the current flowing through the current mirrors can be varied such that the output impedance can also be varied for the required gain.

This research article provides a broad overview of the applications of TIA for NIRS and the different types of TIA and their specific applications in section 1. Section 2 describes the novel low-current input TIA design and circuit. Section 3 explains the findings of the novel TIA and compares its performance with those of existing circuits. Finally, Section 4 concludes the paper.

2. Proposed ultra-low input current TIA architecture

A trans-impedance amplifier for low input current detection for NIRS wearable healthcare devices, such as non-invasive glucometers and pulse oximeters, was designed and implemented in this study. The block diagram in figure 1 illustrates the entire architecture of the proposed TIA. The photocurrent I_{PD} from the photodiode is modeled as a current source connected to the input terminal of the first-stage amplifier with a capacitor C_{PD} connected in parallel with the current source. The first-stage amplifier amplifies this photocurrent and converts it to a few millivolts. The first-stage output is denoted by V_x . The output voltage from

the first stage goes to the second-stage amplifier and is further amplified to a few hundred millivolts. The second-stage output is denoted as V_{out} .

The output voltage of the second-stage amplifier is connected to the positive input of the comparator in the feedback loop. Another terminal of the comparator was connected with the 900mV as a reference voltage. The comparator output controls the selected line of the 2×1 multiplexer. The input terminals of the multiplexer are connected to the feedback resistors R_{f1} (1G Ω -10G Ω) and R_{f2} (500 M Ω -5 G Ω) of the first-stage amplifier. One of the feedback resistors is selected based on the comparator output.

The proposed TIA was implemented using a two-stage amplifier. A modified single-ended differential amplifier that provides a 180 dB Ω trans-impedance gain is the first stage, and a modified telescopic cascode amplifier with high output impedance is the second stage which contributes 59.86 dB Ω gain. This TIA can detect and amplify a very ultralow-input current in the range of 1 pA to 10 pA. A novel automatic saturation mitigation circuit was implemented using a comparator and 2×1 Mux. The output impedance of the first-stage amplifier and second-stage amplifier is varied by external current sources I_{1bias} and I_{2bias} that provide the necessary bias currents, respectively. Variable current mirrors were connected in parallel to the modified current mirrors of the first-and second-stage amplifiers. The output resistance of the variable-current mirrors can be varied by varying the external bias currents. The output impedance of the variable-current mirror was inversely proportional to the bias current. The output resistance of the variable current mirror is in the region of a few kilohms when the bias current is within 1 mA. Conversely, the output resistance of the simple current mirror was in the region of a few gigaohms when the bias current was 1 nA.

A larger bias current resulted in a low-resistance parallel path in the proposed current mirrors. Hence, the output impedance of the modified current mirrors can be reduced because of their low parallel resistance. Similarly, a low bias current provides a high-resistance parallel path in the modified current mirrors. Hence, the output impedance of the proposed current mirrors can be increased such that current flows in the normal path. Hence, the proposed current mirrors operate normally with their actual output impedance. Hence, by changing the external bias currents of the variable-current mirror, the gain of both amplifiers can be varied by changing the output impedance of the amplifier.

2.1 First stage: proposed differential amplifier

The first stage was implemented using a modified differential amplifier with a modified current mirror to provide high output impedance to achieve high gain to amplify the

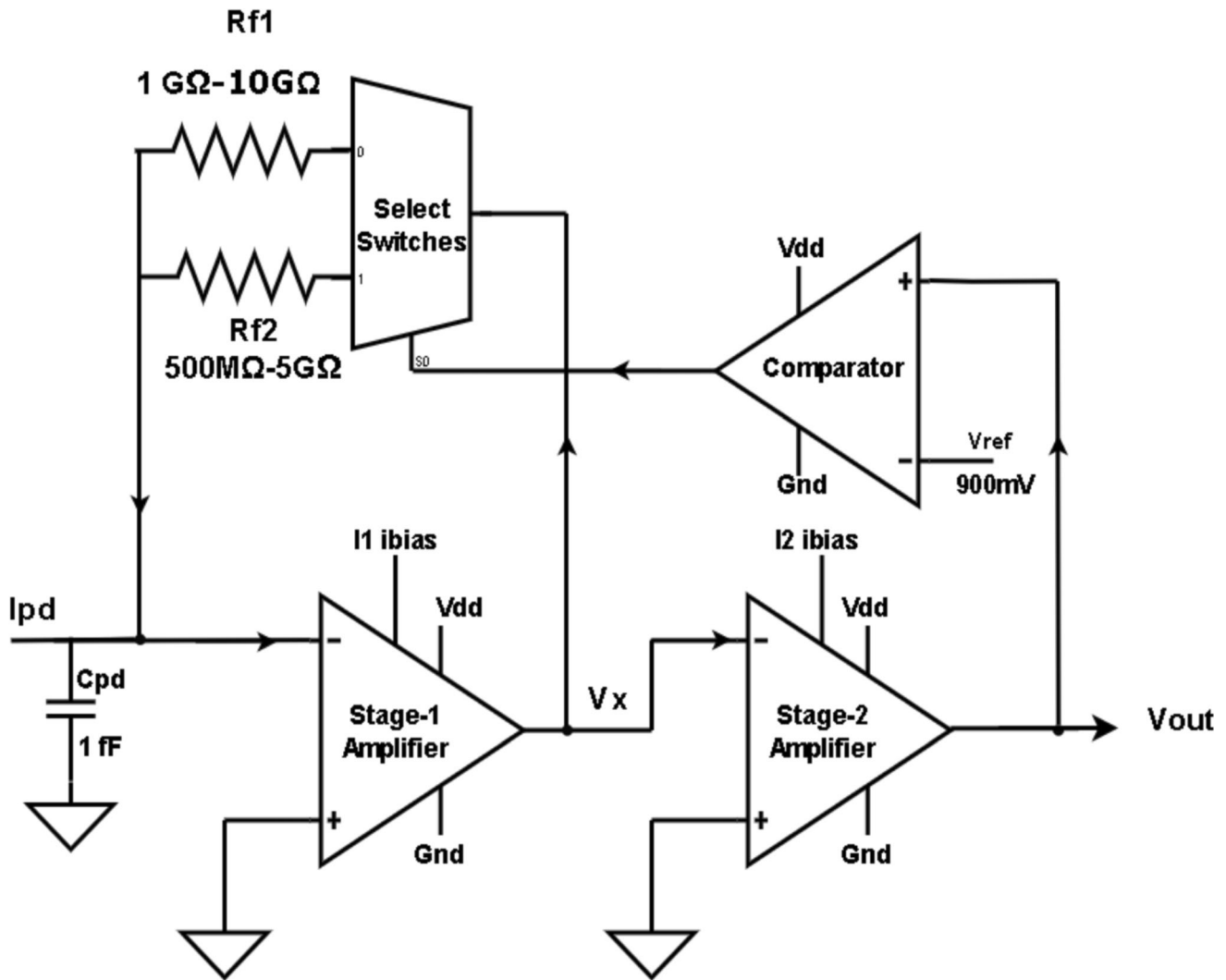


Figure 1. Block Diagram of the Proposed Low Input Current TIA.

ultralow input current in the range of a few millivolts. The proposed single-ended differential amplifier was realized as a high-gain trans-impedance amplifier to detect ultra-low input current signals in the range of 1 pA to 10 pA. The first stage was implemented using a single-ended differential pair with feedback resistors R_{f1} and R_{f2} with values of $1\text{ G}\Omega$ - $10\text{ G}\Omega$ and $500\text{ M}\Omega$ - $5\text{ G}\Omega$, respectively. When the input current was 1 pA, the $10\text{ G}\Omega$ feedback resistor value was connected. When the input current was 10 pA, a $1\text{ G}\Omega$ feedback resistor was connected. The resistors are external. The feedback resistors R_{f1} and R_{f2} can be varied to detect a wide range of input currents from the photodiode generated by the low-intensity IR signals. By changing the value of the feedback resistor in the first stage, various gain levels can be achieved, and different amplitudes of the input current can be detected and amplified.

Figure 2 shows the schematic of the proposed TIA. When the output voltage V_x from the first stage across transistor

M_{F1} is greater than the threshold voltage ($V_{thM_{F1}}$), it is in the active region and starts to amplify the input signal. The transistors M_{F3} – M_{F8} are in saturation and work as the modified current mirror, which provides a high output impedance to stage-1.

The output impedance of stage-1 is calculated using Equation (1). The overall output resistance provided by the modified current mirror can be determined by calculating the values of the transconductance (g_m) and output resistance (r_o) of the corresponding transistors.

Output Impedance of first stage

$$= (\mathbf{g}_{mF3} \mathbf{x} \mathbf{r}_{0F3} \mathbf{x} \mathbf{r}_{0F1}) || (\mathbf{g}_{mF5} \mathbf{x} \mathbf{r}_{0F5} \mathbf{x} \mathbf{r}_{0F7}) \quad (1)$$

The first-stage gain of the proposed TIA can be calculated using Equation. The gain of the first-stage amplifier can be calculated by calculating the values of the transconductance (g_m) and output resistance (r_o) of the corresponding transistors.

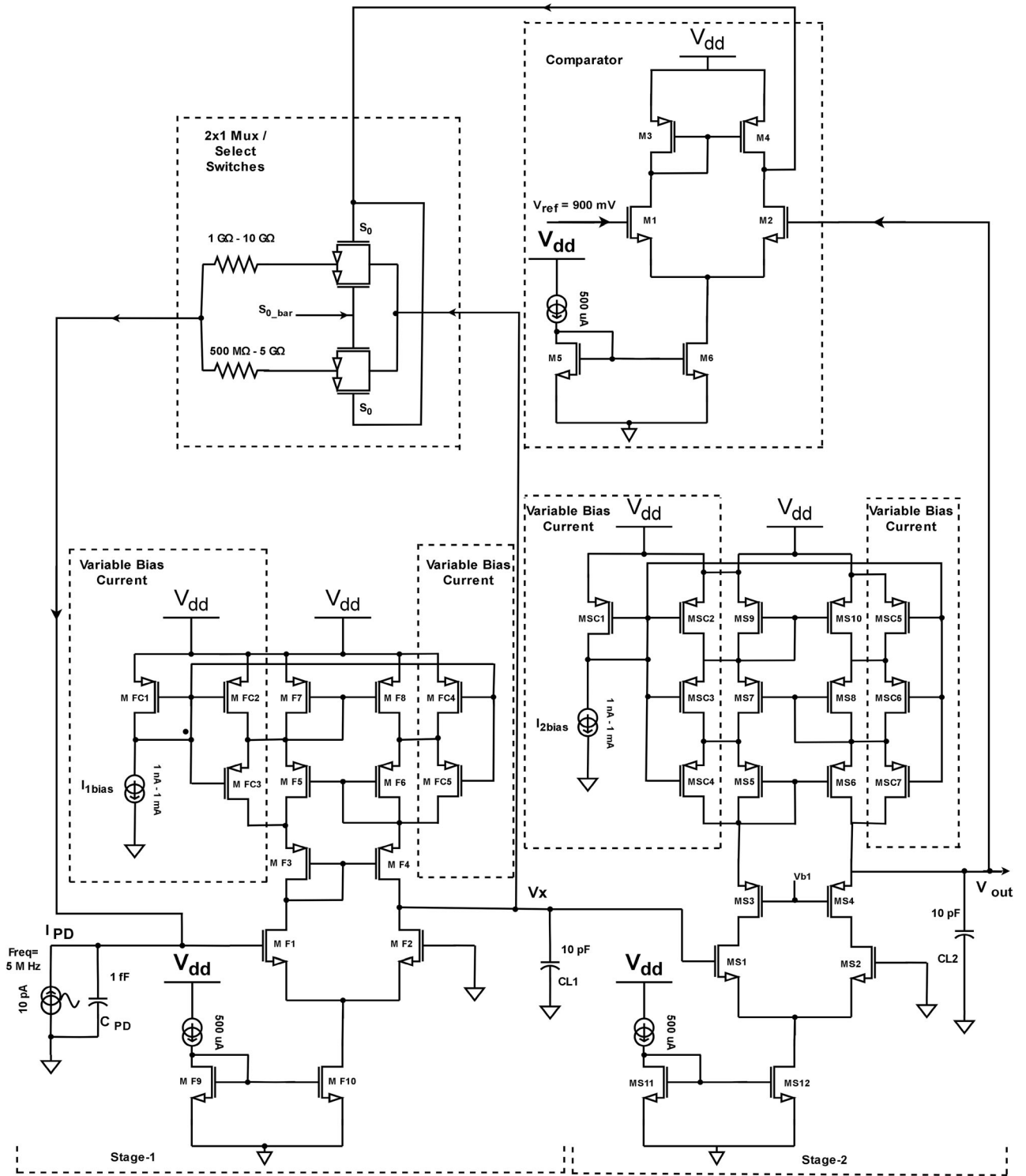


Figure 2. Schematic Diagram of the Proposed Low Input Current TIA.

$$\text{Gain of the First Stage} = -g_{mF1} \times [(g_{mF3} \times r_{OF3} \times r_{OF1}) || (g_{mF5} \times r_{OF5} \times r_{OF7})]$$

(2)

$$\text{Transconductance } (g_m) = \sqrt{\mu_n \times C_{ox} \times (W/L) \times I_D} \quad (3)$$

$$\text{Drain Current } (I_D) = (1/2) \times \mu_n \times C_{ox} \times (W/L) \times (V_{gs} - V_{th})^2 \quad (4)$$

The transconductance and drain current of the transistors were calculated using Equations (3) and (4), respectively:

The transconductance can be calculated by applying the mobility values of the electrons (μ_n), gate capacitance (Cox), width of the transistor (W), length of the transistor (L), and drain current (I_D) of the transistors.

The transistor sizes were calculated based on the requirement of providing a high output impedance to achieve a 180 dB gain from the first stage. The calculated transistor sizes are listed in table 1. M_{F1} – M_{F10} represent the transistors of the first-stage amplifier.

2.2 Second stage: proposed telescopic cascode amplifier

The second stage was implemented using a proposed telescopic cascode amplifier to provide further boosting of the weak signal, which is in the range of a few millivolts to a few hundred millivolts. The proposed telescopic cascode amplifier has high gain, moderately high input impedance, high output impedance, and high bandwidth. The proposed telescopic cascode configuration improves the input-output isolation by eliminating the Miller effect, which results in a much higher bandwidth. The proposed telescopic cascode amplifier has a very high output impedance, which provides a high gain and swing to the second-stage output voltage (V_{out}).

When $V_x \leq V_{b1} - V_{thMS4}$, transistor M_{S4} is in the triode region and the other transistors are in the saturation region. When $V_{b1} - V_{thMS4} \leq V_x \leq V_{b1} - (V_{gsS4} - V_{thMS2})$, M_{S2} and M_{S4} are saturated. When $V_x \geq V_{b1} - (V_{gsS4} - V_{thMS2})$, $MS1$ and $MS2$ are in the triode region while $MS4$ is in saturation. Transistors M_{S5} – M_{S10} were saturated and acted as a constant-current source. Transistors M_{S5} – M_{S10} work as active loads to the second-stage output and provide a high output impedance to the second stage. Transistors M_{S11} – M_{S12} formed a current mirror to provide the necessary bias current to the telescopic cascode amplifier. The calculated transistor sizes for the second-stage telescopic amplifier are presented in table 2. The values of the passive components are listed in table 3. The dimensions of the comparators are presented in table 4. The output impedance of the proposed telescopic cascode amplifier was calculated using Equation (5). The second-stage gain of the proposed TIA can be calculated using Equation.

Table 1. Transistor Sizing of First Stage Amplifier.

Transistor	Size W/L ($\mu\text{m}/\mu\text{m}$)
M_{F1} – M_{F2}	10/0.045
M_{F3} – M_{F4}	17/0.045
M_{F5} – M_{F6}	24/0.045
M_{F7} – M_{F8}	30/0.045
M_{F9} – M_{F10}	38/0.045

Table 2. Transistor Sizing of Second Stage Amplifier.

Transistor	Size W/L ($\mu\text{m}/\mu\text{m}$)
M_{S1} – M_{S2}	8/0.045
M_{S3} – M_{S4}	14/0.045
M_{S5} – M_{S6}	20/0.045
M_{S7} – M_{S8}	24/0.045
M_{S9} – M_{S10}	32/0.045
M_{S11} – M_{S12}	32/0.045

Output Impedance of stage2

$$= (g_{ms3} \times r_{0s3} \times r_{0s1}) || (g_{ms5} \times r_{0s5} \times r_{0s7}) || (g_{ms7} \times r_{0s7} \times r_{0s9}) \quad (5)$$

Gain of the second stage

$$= -g_{ms1} \times [(g_{ms3} \times r_{0s3} \times r_{0s1}) || (g_{ms5} \times r_{0s5} \times r_{0s7}) || (g_{ms7} \times r_{0s7} \times r_{0s9})] \quad (6)$$

2.3 Novel saturation mitigation technique

Saturation in the TIA is a serious concern when a large input current is applied to the TIA with a high gain. The TIA is designed to amplify a certain range of currents for specific applications. When the output voltage reaches saturation, the amplifier becomes unresponsive to changes in the input current, because it reaches the supply voltage. As long as the input current exceeds the specified limit, the TIA output will be saturated and the TIA will be useless for any signal processing. Hence, it is important to maintain a specified range of input currents or use a saturation mitigation technique to address this issue.

Several approaches have been implemented to enhance the dynamic range of TIAs in the literature. One approach is to use voltage amplifiers as the next stage and split the TIA gain between two or more stages [25]–[29]. The TIA can become saturated for larger input currents; hence, it is advisable to lower the feedback resistance to reduce the gain of the TIA [30] Another technique implements a

Table 3. Component Values.

Components	Values
R_{f1}	1 G Ω –10 G Ω
R_{f2}	500 M Ω –5 G Ω
C_{L1}	10 pF
C_{L2}	10 pF
I_{bias}	500 μA
V_{b1}	0.5 V

Table 4. Transistor Dimensions of Comparator.

Transistor	Size W/L ($\mu\text{m}/\mu\text{m}$)
M ₁ -M ₂	3.6/0.045
M ₃ -M ₄	3.6/0.045
M ₅ -M ₆	7.2/0.045

logarithmic TIA using a nonlinear feedback network containing a transistor or diode. The input overload current of such a TIA can be significantly increased by operating over multiple decades of the input current [31].

A popular technique for increasing the dynamic range of TIAs is the use of an automated gain control (AGC) mechanism [32]–[36]. The control loop that measures and controls the gain of the TIA's output voltage is called AGC. As a result, it adjusts its feedback resistor or variable input current limiter circuit to regulate the gain of the TIA. Numerous commercial programmable gain TIA devices have available [37].

To overcome the limitations of saturation mitigation techniques used in the literature, a novel technique was implemented to avoid the saturation scenario of the second-stage amplifier. The V_{ref} input terminal of the comparator was connected at 900mV. When the input of the comparator crosses 900 mV, the output of the comparator will be binary '1' otherwise it will be binary '0.' When the input current was approximately 1 pA, the feedback resistor was set as 10 G Ω . In this scenario, the output of the second-stage amplifier is 900 mV. If the input current slightly increases beyond 1pA, then the second-stage amplifier becomes saturated. Similarly, when the input current was approximately 10 pA, the feedback resistor was set as 1 G Ω . In this scenario, the output of the second-stage amplifier is 900 mV. If the input current slightly increases beyond 10pA, then the second-stage amplifier becomes saturated. To avoid such a scenario, a novel feedback control loop for saturation mitigation is implemented in the proposed TIA.

The feedback loop consisted of a comparator and two programmable switches to avoid saturation. The programmable switches were connected to the feedback loop of the first stage with two feedback resistors with values of 1 G Ω -10 G Ω and 500 M Ω 5G Ω as shown in the block diagram. Feedback resistor 1 G Ω -10 G Ω is connected to '0' (binary zero) input and the 500 M Ω - 5 G Ω is connected to '1' (binary one) input of switches. Based on the 'select' signal of the switch, one of the feedback resistors was connected to the feedback loop of the first-stage amplifier.

The reference voltage of the comparator is fixed at 900 mV. When the output voltage of the second stage amplifier is less than 900 mV, then the comparator output will be '0' (binary zero) and the switch 'select' signal will be '0.' Hence, the feedback resistor connected to the '0' input of

the switch is active in the feedback loop, and the other resistor is open-circuited. Similarly, when the output voltage of the second stage amplifier is more than 900 mV, then the comparator output will be '1' (binary one) and the switch 'select' signal will be '1.' Hence the feedback resistor connected to the '1' input of the switch will be active in the feedback loop and the other resistor will be open-circuited.

The proposed TIA can handle twice the input current without saturating the second-stage amplifier. Hence, this novel saturation-mitigation arrangement avoids the saturation issue of the second-stage amplifier. By selecting suitable feedback resistors, this novel saturation-mitigation arrangement can provide the required gain without saturating the second stage. The proposed TIA output never saturates because the reference voltage of the comparator is fixed at 900 mV for a supply voltage of 1V.

A comparison of the different saturation mitigation techniques is presented in table 5. Memristor-based Automatic Gain Control [38] is another saturation mitigation technique used for various amplifiers. A periodic reset of the readout circuits to cancel the input-referred offset voltages [39] and a self-regulating DC photocurrent loop [40] can also be used to prevent the saturation of the TIA. Resistor-feedback-based TIA active-feedback current-based saturation mitigation [41] is another popular saturation mitigation technique. A major drawback of capacitive feedback TIA [42] is that the charge that builds up across the capacitor may cause the amplifier's output voltage to become saturated. Two methods are frequently used to circumvent this restriction. The first approach, known as the discrete-time (DT) strategy, removes the charge stored in the feedback capacitor by periodically adding a reset switch. The continuous-time (CT) method is another strategy that eliminates the baseline current by adding a DC cancellation circuit to avoid output saturation. From the comparative analysis, it is evident that our proposed TIA supports the lowest input current of 1pA–10 pA with a high gain of 236.86 dB Ω . Comparator-based saturation mitigation is a novel technique that has not yet been presented in the literature.

2.4 Variable current mirror for output impedance control

The output impedances of the first- and second-stage amplifiers can be varied by the external current sources $I_{1\text{bias}}$ and $I_{2\text{bias}}$ that provide the necessary bias currents, respectively. Variable current mirrors are connected in parallel to the modified current mirrors of the stage-1 and stage-2 amplifiers. The output resistance of the variable-current mirror can be varied by varying the external bias current. The output impedance of the variable-current mirror was inversely proportional to the bias current. When the bias current was 1 mA, the output resistance of the

Table 5. Saturation mitigation techniques.

Description	[38]	[39]	[40]	[41]	[42]	This Work
Input Current Range	−1 nA to +1 nA	±200 pA and ±20 nA	2.7 μ A to 15 μ A	±1 μ A	±200 pA −2 nA	1 pA to 10 pA
Output Voltage Range (V)	−1 V to +1 V	±450 mV	1.251	1	800 mV	100 mV to 900 mV
Transimpedance Gain (dB Ω)	80	187	63.5	48	206	236.86
Amplifier Stages	2	3	2	3	2	2
Architecture	Memristor Based AGC	Switched Capacitor Amplifier	Dual-loop TIA	Resistive Feedback	Capacitive Feedback	Differential Amplifier
Saturation	Automatic Gain Control	Digital offset compensation	self-regulating DC Current	Active current feedback	Continuous	Comparator
Mitigation Technique					& Discrete Time Reset	based Gain Control
Application	Bio-sensing	Microfluidic devices	Bio-sensing	ECG	Bio-Sensors	Bio-Sensors

variable current mirror was in the range of a few kilohms. However, when the bias current was in the range of 1 nA, the output resistance of the simple current mirror was in the range of a few gigaohms. The variable or tunable bias current sources are connected in parallel with the output impedances of the first- and second-stage amplifiers.

MOSFETs M_{F3} – M_{F8} contribute to the output impedance of the first-stage amplifier. MOSFETs M_{FC3} – M_{FC5} are from the variable current source and are in parallel with the output impedance of the first-stage amplifier. All parallel transistors in the first stage shared the same bias current I_{1bias} . Similarly, MOSFETs M_{S5} – M_{S10} contribute to the output impedance of the stage-2 amplifier. MOSFETs M_{SC2} – M_{SC7} are from the variable current source, and they are in parallel with the output impedance of the stage-2 amplifier. All parallel transistors in the second stage share the same bias current I_{2bias} .

The proposed TIA is mainly designed to detect and amplify an ultralow input current of 1 pA to 10 pA. However, this TIA can be used to detect and amplify higher currents in the range of a few picoamperes to milliamperes by reducing the gain required for the input current to be amplified. The required gain can be varied by changing the output resistances of the first- and second-stage amplifiers. The output resistance of the first stage could be varied by changing the I_{1bias} current of the first stage. The required amount of gain in the first stage was set. Similarly, the required gain in the second stage can be varied by varying the I_{2bias} current in the second stage. By changing the gain settings of both stages, any range of input currents from a few picoamperes to milliamperes can be obtained.

3. Results and discussion

The proposed ultra-low input current sensing TIA was designed using the GPDK 45 nm technology node, and the schematic was simulated using the Cadence Analog Design Environment (ADE) with Specter as the simulator. The input photocurrent I_{PD} can be varied from 1 to 10 pA with a signal frequency of 5 MHz. The feedback resistor was selected based on the amplitude of the input current and the input capacitance was set to 1 fF. The supply voltage of the TIA is 1 V. The simulation and operating temperatures were set to 27 °C. A transient simulation was performed to analyze the output voltage V_{out} for different levels of the input photocurrent.

Case-1: When the input current is 1 pA, a 10 G Ω feedback resistor is selected, and the corresponding output voltage (V_x) of the first-stage amplifier is 10 mV.

Case-2: When the input current is 10 pA, a 1 G Ω feedback resistor is selected, and the corresponding output voltage (V_x) of the first-stage amplifier is 10 mV.

The sample calculations were as follows: The output voltage of the first stage of the TIA was calculated using

Equation (7). The Trans-Impedance gain of the TIA and the bandwidth are calculated using Equations (8) and (9), respectively.

$$\text{Output Voltage of the TIA Stage} - 1(V_x) = I_{PD} \times R_{f1} \quad (7)$$

3.1 V_x Sample calculations:

$$\text{Case-1: } I_{PD} = 1 \text{ pA} = 1 \times 10^{-12} \text{ R}_f = 10 \text{ G}\Omega = 10 \times 10^9$$

$$V_x = 1 \times 10^{-12} \times 10 \times 10^9 = 10 \times 10^{-3} = 10 \text{ mV}$$

$$\text{Case-2: } I_{PD} = 10 \text{ pA} = 10 \times 10^{-12} \text{ R}_f = 1 \text{ G}\Omega = 1 \times 10^9$$

$$V_x = 10 \times 10^{-12} \times 1 \times 10^9 = 10 \times 10^{-3} = 10 \text{ mV}$$

$$\text{TransimpedanceGain} = 20 \times \log_{10} \left(\frac{V_x}{I_{PD}} \right) \quad (8)$$

$$\text{Bandwidth} = 1 / (2\pi \times C_{PD} \times Z(0)_{in}) \quad (9)$$

The transimpedance gain of the first stage of the TIA was 180 dB Ω . Where I_{PD} is the input current from the photodiode, C_{PD} is the input capacitance, R_{f1} is the feedback resistor, V_x is the output voltage of the first stage of the TIA, and $Z(0)$ is the input impedance of the TIA.

The TIG of the first stage of TIA was 180 dB Ω . Where I_{PD} is the input current from the photodiode, C_{PD} is the input capacitance, R_{f1} is the feedback resistor, V_x is the output voltage of the first stage of the TIA, and $Z(0)$ is the input impedance of the TIA. The simulation waveform of the proposed TIA input current for the first-stage amplifier is shown in figure 3. The input current is 10 pA. The maximum gain that can be achieved in the first stage is 180 dB Ω only in the present scenario. The output voltage of the first stage was approximately 10 mV when the input current was 10 pA, and the feedback resistor was 1 G Ω . Similarly, the output voltage of the first stage is approximately 10 mV when the feedback resistor is 10 G Ω , and the input current is 1 pA from the calculation using Equation (7). Hence, a second-stage amplifier is required to boost the weak signal into a strong signal. The second stage amplified the 10 mV output from the first stage to 900 mV with a gain of 59.86 dB. Figure 4 shows the input and output voltages of the proposed second-stage telescopic cascode amplifier.

The maximum achieved output voltage was 900mV for a given ultralow input current of 10 pA. The maximum achieved trans-impedance gain was 239.86 dB Ω and the -3 dB bandwidth was 10 MHz for the above-mentioned simulation setup.

The linearity of the TIA can be examined based on the transverse characteristics of the input and output. The linear behavior of the proposed TIA was tested by varying the input current from 1 to 10 pA while maintaining different gain settings. The maximum output of 10 pA when the feedback resistor is 0.5 G Ω is 450 mV. Similarly, the maximum output at 10 pA when the feedback resistor was 1 G Ω was 900 mV. It is evident from the graph that these two

graphs obey linearity. This TIA is designed to handle a maximum output of 900 mV for an input current ranging from 1 pA to 10 pA. The maximum achievable trans-impedance gain for a 1 G Ω feedback resistor is 239.86 dB Ω . The maximum input current could be 10 pA to obtain a maximum output of 900 mV without any saturation or linearity issues. If the TIA input exceeds 10 pA when the gain setting is 239.86 dB Ω the linearity of the TIA will be affected. Similarly, if the gain setting is more than 239.86 dB Ω when the feedback resistor is 1.5 G Ω , an input current of more than 7 pA will affect the linearity of the TIA, leading to saturation. Hence, this TIA uses 1 G Ω and 0.5 G Ω resistors in the proposed architecture to maintain full linearity, and the saturation is also mitigated. The linearity of the proposed TIA is shown in figure 5.

AC simulation and analysis of the proposed TIA were performed from 10 Hz to 100 MHz. The maximum bandwidth at -3 dB gain was 10 MHz when the gain reaches 236.86 dB Ω . The Unity Gain Bandwidth (UGB) of this TIA was 100 MHz, and the phase margin was 72°. Figure 6 shows the frequency-response plot of the gain. The transimpedance gain is inversely proportional to the operating temperature. When the operating temperature increased gradually, the transimpedance gain decreased slightly owing to the decrease in the transconductance of the transistors. The effect of temperature on transimpedance gain is shown in figure 7. At room temperature, the trans-impedance gain was 239.86 dB Ω . At 50 °C, the gain decreases to 237.46 dB Ω . When the temperature was 75 °C, the transimpedance gain was 235.08 dB Ω . At 100 °C, it reaches 232.73 dB Ω . Temperature affects the performance of TIA.

The variations in the performance parameters, such as the trans-impedance gain and bandwidth, are analyzed using Monte Carlo simulations. To analyze the effect of mismatch, Process, Voltage and Temperature (PVT) variations on the transimpedance gain and bandwidth, 100 samples were obtained. Figures 8(a) and (b) show the Monte Carlo simulation results for the transimpedance gain and bandwidth, respectively. They show that the average trans-impedance gain due to mismatch and PVT variation is 197.74 dB Ω and the standard deviation (σ) is 69.87 dB Ω . Similarly, the average bandwidth was 8.93 MHz and the standard deviation (σ) was 1.23 MHz.

The impact of the variable bias current and the corresponding change in the gain of the first stage are shown in Figure 9.a, and the change in the gain of the second stage is shown in Figure 9.b. When the I_{1bias} and I_{2bias} currents are zero '0,' no bias current flows through the variable current mirrors of the first and second stages. Hence, there was no change in the output impedances of the first and second stages. Both the first- and second-stage amplifiers provided maximum gain. However, when the I_{1bias} and I_{2bias} currents are 1nA, the effective resistance provided by the bias current is in the range of a few gigaohms, in parallel with the output impedances. Hence, the effective output impedance is decreased by 5% approximately so that the TIG of the

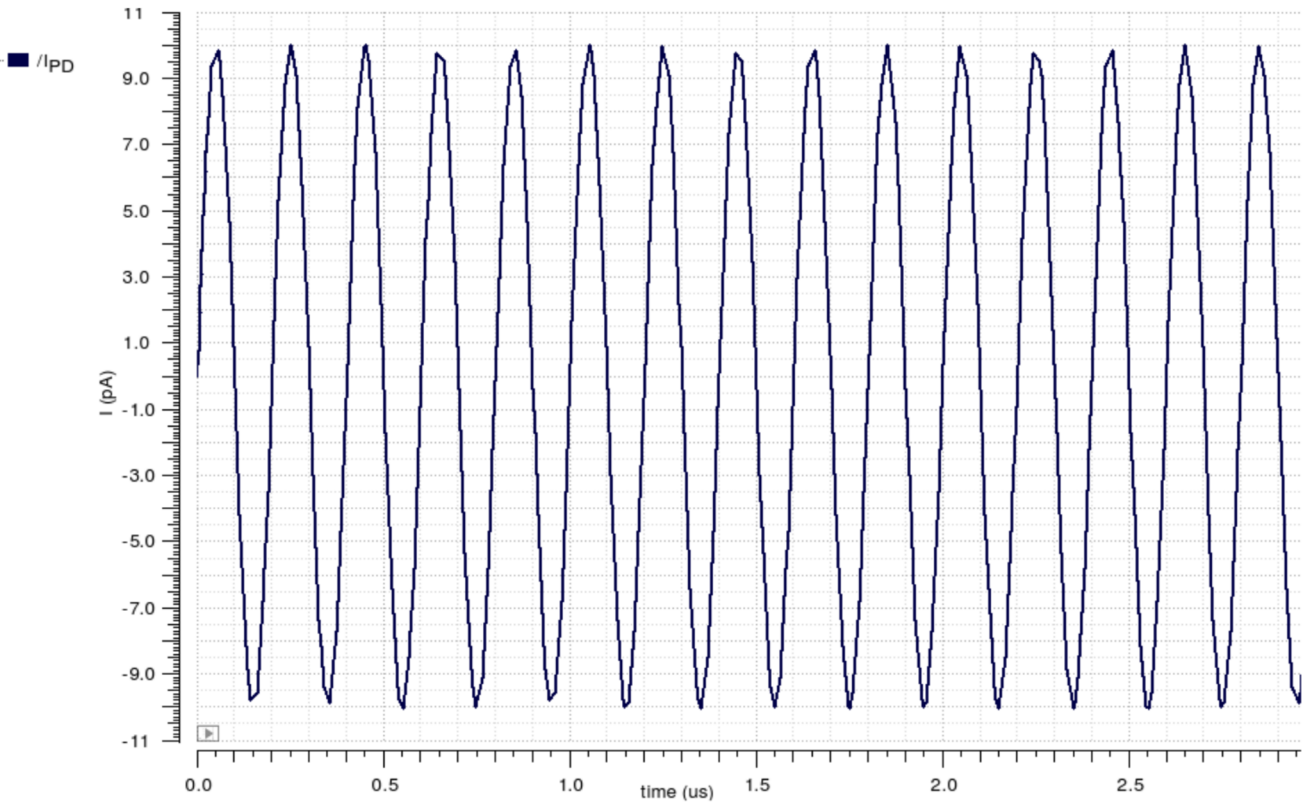


Figure 3. Input current of Stage 1 TIA.

first-and second-stage amplifiers is almost reduced by 5% from the actual gain.

The bias current sources $I_{1\text{bias}}$ and $I_{2\text{bias}}$ were varied from 1nA to 1 mA to analyze the impact on the TIG. When $I_{1\text{bias}} = 0$ A, the TIG of the first stage is the maximum and at is 180 dB Ω . When the $I_{1\text{bias}}$ current was increased to 1nA, 1 μ A and 1mA then the TIG of the first stage decreased to 171, 162, and 153 dB Ω , respectively. Similarly, when $I_{2\text{bias}} = 0$ A, the transimpedance gain of the second stage is at its maximum, and it is 59.86 dB Ω . When $I_{2\text{bias}}$ current is increased to 1nA, 1 μ A and 1mA then the trans-impedance gain of the second stage decreases to 56.8 dB Ω , 53.7 dB Ω and 50.8 dB Ω respectively. By varying the $I_{1\text{bias}}$ and $I_{2\text{bias}}$ currents of the proposed variable current circuit, a variety of variable gains can be achieved. Figure 10 illustrates the impact of the $I_{1\text{bias}}$ and $I_{2\text{bias}}$ currents on the overall TIG of the proposed TIA.

Sample Calculation of Variable-Current Mirror Output Resistance

$$\text{Current Mirror Output Resistance } (R_{\text{out}}) = \frac{L}{(\lambda_L \times I_{\text{bias}})} \quad (10)$$

where,

L – Lenth of the MoSFET (μm)

λ_L – Channel Length Modulation of the device ($\mu\text{m/V}$)

If $L = 10 \mu\text{m}$; $\lambda_L = 0.1 (\mu\text{m/V})$ and $I_{\text{bias}} = 1\text{nA}$

$$R_{\text{out}} = 10 \times 10^{-6} / (0.1 \times 10^{-6} \times 1 \times 10^{-9})$$

$$R_{\text{out}} = 100 \times 10^9 = 100 \text{ G}\Omega$$

When $I_{1\text{bias}} = 0$ A and $I_{2\text{bias}} = 0$ A, the trans-impedance gain of the second stage is a maximum at 239.86 dB Ω . When $I_{1\text{bias}}$ and $I_{2\text{bias}}$ currents are increased to 1nA, 1 μ A and 1mA then the overall trans-impedance gain decreases to 227.73 dB Ω , 215.87 dB Ω and 203.88 dB Ω respectively. From the analysis, it is evident that the output impedance decreases as the bias current increases; hence, the trans-impedance gain is inversely proportional to the bias current. It is possible to vary the transimpedance gain of the proposed TIA by changing the bias current of the variable-current impedance circuit. The output resistance of the variable-current mirror can be calculated using Equation (10).

In the first stage, the TIA gain was significantly influenced by the feedback resistor. The output voltage V_x of the first-stage TIA was analyzed by varying the feedback resistor from 1 to 10 G Ω and fixing the input current in the range of 1, 2.5, 5, and 10 pA. The effect of the feedback resistor on the first-stage output is shown in Figure 11. From this analysis, it is evident that the output voltage V_x is directly proportional to the feedback resistor. When $I_{\text{PD}} = 1\text{pA}$ and $R_f = 10 \text{ G}\Omega$, the first-stage output is 10mV. Similarly, the first-stage output can be fixed at 10mV with

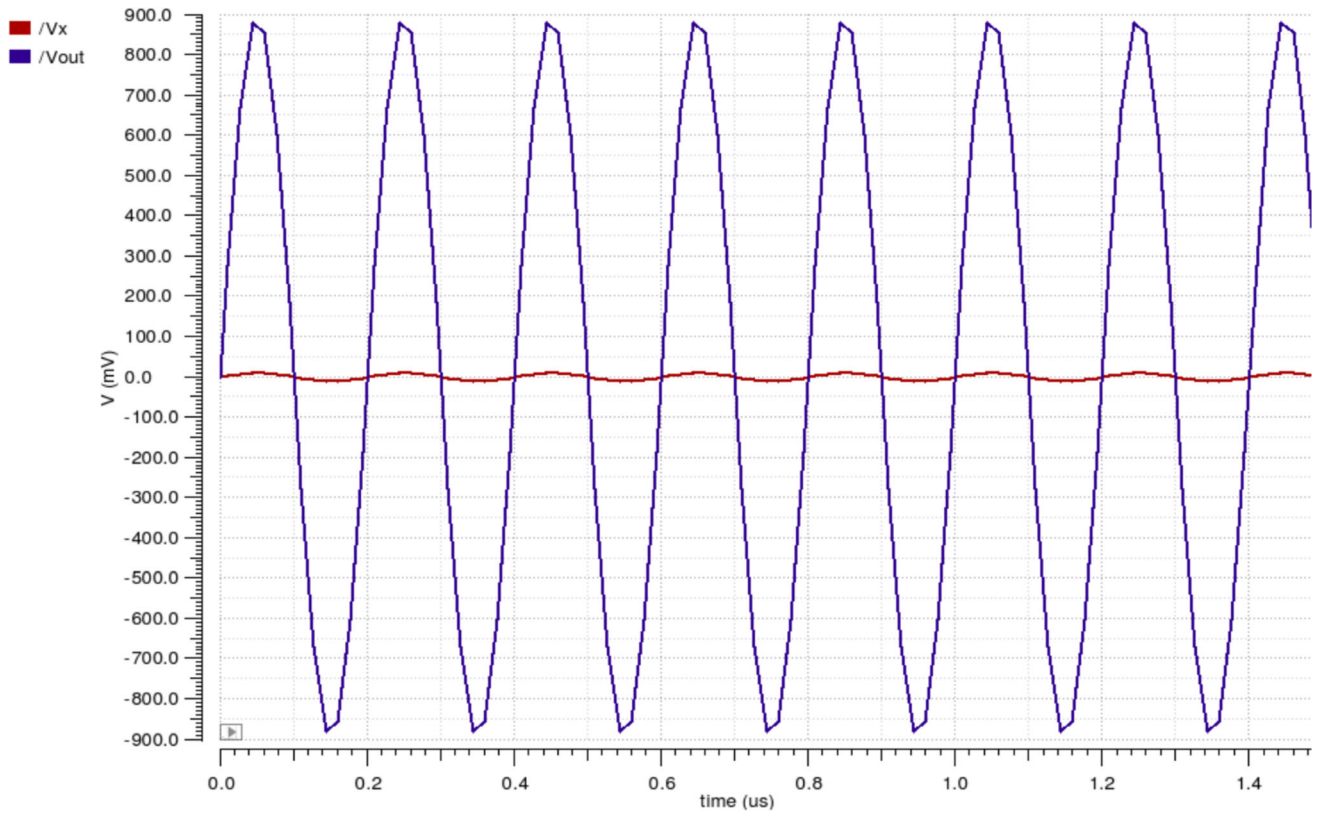


Figure 4. Input and Output voltages of stage-2 Amplifier.

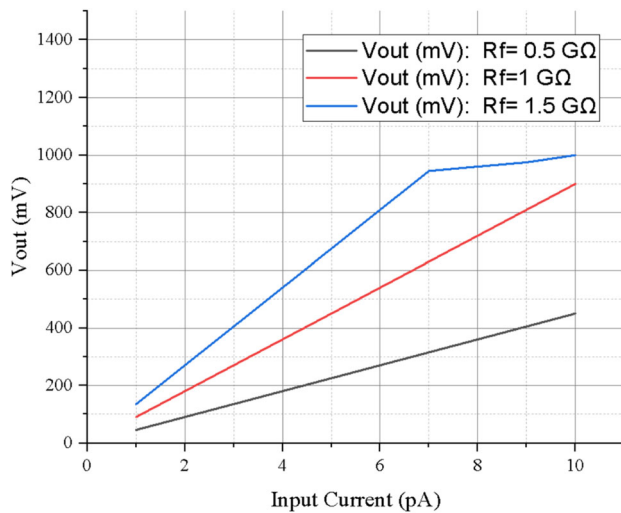


Figure 5. Linearity Check (Input-Output Transverse Characteristics).

different combinations of the input current and feedback resistance. Possible combinations are highlighted in the graph by dots.

When $I_{PD}=5$ pA and $R_f=2$ G Ω , the first-stage output is 10mV. When $I_{PD}=10$ pA and $R_f=1$ G Ω , the first-stage output is 10mV. The highlighted dots in figure 11 show the safe

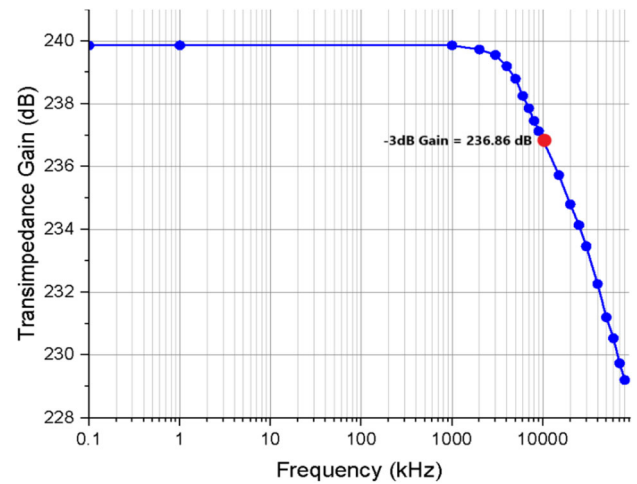


Figure 6. Frequency response of the proposed low input current TIA.

output V_x range of the first-stage amplifier, below which there is no saturation issue in the second stage. If the value of V_x is greater than 10 mV, the second-stage amplifier is saturated. This saturation issue is addressed by the proposed saturation mitigation circuit in the proposed TIA.

The effect of the feedback resistor on the overall TIG was observed by varying the feedback resistor. The value of

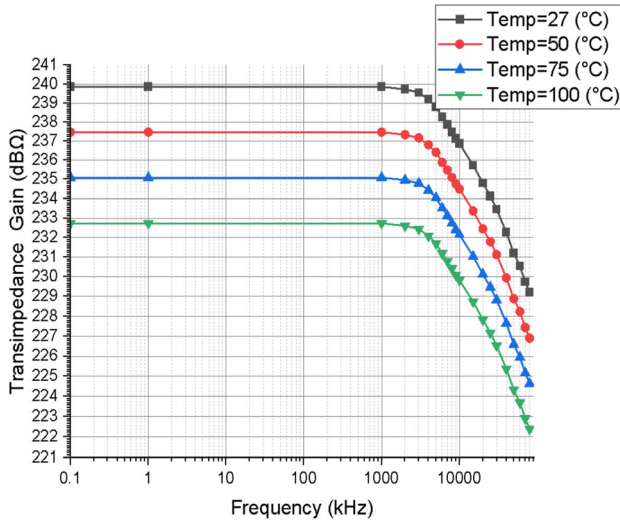


Figure 7. Frequency response of the Transimpedance Gain with Temperature.

the feedback resistor is changed from 100 MΩ to 1 GΩ, and the variation in the trans-impedance gain is observed and plotted in Figure 12. From the analysis, it is evident that the trans-impedance gain at 100 MΩ is 219.86 dBΩ and it reaches 239.86 dBΩ when the feedback-resistor's value is 1 GΩ. The required transimpedance gain can be achieved by varying the value of the feedback resistor. The variation in transimpedance gain is directly proportional to the logarithmic function of the feedback resistor.

The influence of the feedback resistor on the bandwidth of the proposed TIA is analyzed, and the results are plotted. The value of the feedback resistor was varied from 100 to 1000 MΩ and the results were observed. When the value of the resistor was 100 MΩ, the bandwidth was 11.25 MHz and the bandwidth reached 10 MHz when the feedback resistor was 1000 MΩ. Figure 13 shows a pictorial

representation of the impact of the feedback resistor on bandwidth. The required bandwidth can be achieved by varying the resistor value. The variation in the bandwidth is inversely proportional to the inverse Log_{10} function.

The impact of temperature on the thermal noise was observed by varying the temperature from -40 °C to +125 °C for different bandwidths. 8, 10, and 12 MHz, respectively. The thermal noise is calculated using Equation (11) when the bandwidth of the amplifier is fixed. The amount of thermal noise increases as the temperature increases. Figure 14 shows the impact of temperature and bandwidth on thermal noise. From the simulation results, it is evident that the thermal noise is lower when the operating temperature is lower.

Thermal noise and the figure of Merit (FoM) can be calculated using Equations (11) and (12), respectively.

$$\text{Thermal Noise} = K_B \times T \times B \quad (11)$$

where,

$$K_B - \text{Boltzmann constant} = 1.380649 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$$

T - Temperature (Kelvin)

B - Bandwidth (MHz)

$$\text{Figure of Merit (FoM)} = \frac{\text{Gain (dB}\Omega) \times \text{Bandwidth (GHz)}}{\text{Power (mW)}} \quad (12)$$

The frequency response of the input-referred noise is plotted in Figure 15. The frequency was varied from 10 Hz to 100 MHz to observe the frequency response of input-referred current noise. When the frequency is 10 Hz, the amplitude of the input-referred noise current is 40 fA/√Hz. As the frequency increased, the amplitude of the input-referred current noise decreased and became almost flat after 1 KHz. The input-referred noise current of the proposed TIA at 10 MHz was 12.9 fA/√Hz.

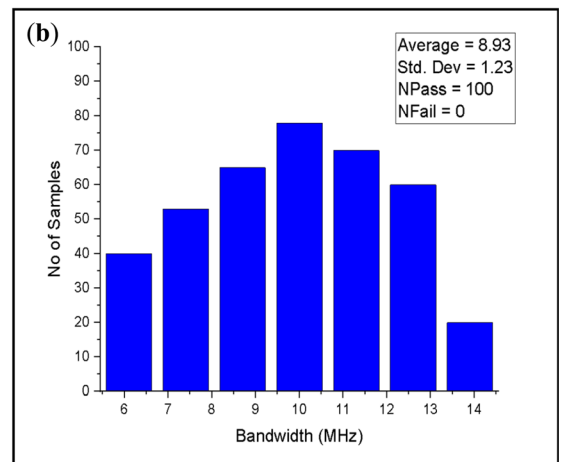
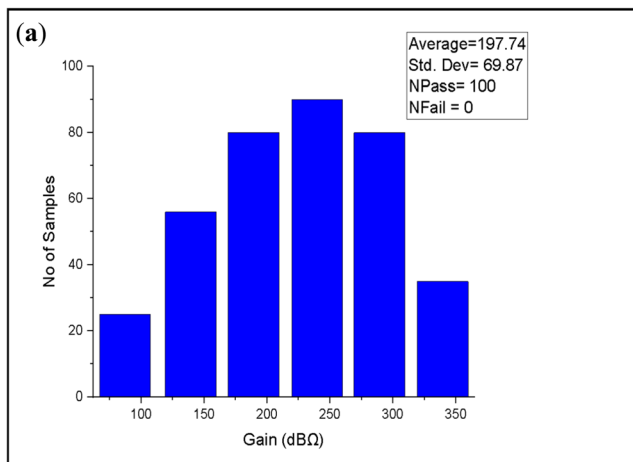


Figure 8. a. MonteCarlo Results of Gain b. MonteCarlo Results of Bandwidth.

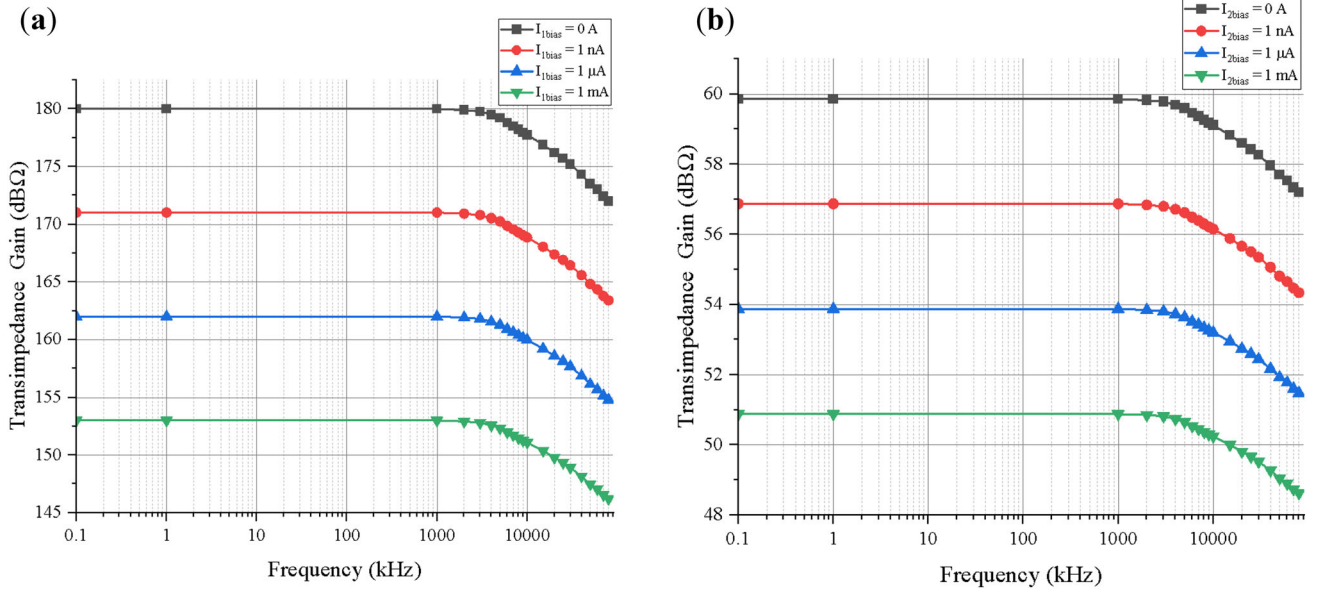


Figure 9. a. I_{bias} vs Transimpedance Gain of First Stage b. I_{bias} vs Transimpedance Gain of Second Stage.

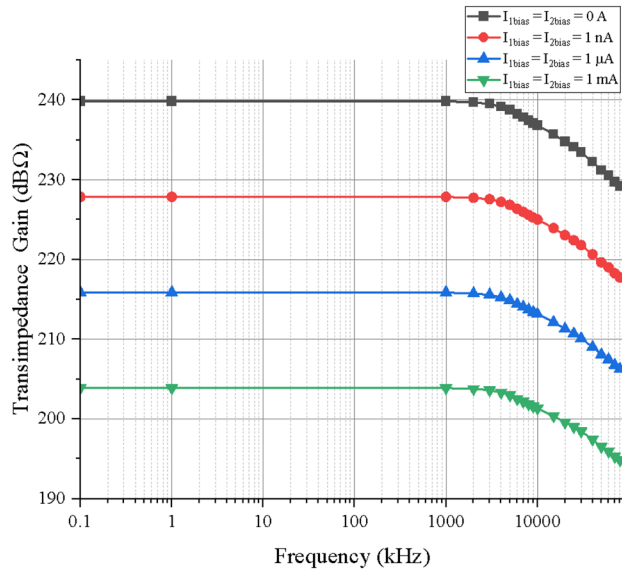


Figure 10. I_{bias} and I_{bias} vs Overall Transimpedance Gain of the proposed TIA.

The input-referred noise current of the proposed TIA can be calculated using Equation (13). By substituting the respective values of g_m , C_{pd} , Bandwidth, and feedback resistors, the input-referred noise of the proposed TIA can be calculated theoretically.

$$I_{n,in}^2 = 4K_B T \left[\frac{(G_m^2 + (2\pi f C_{pd})^2) BW}{(1 - G_m R_f)^2} \right] \quad (13)$$

The frequency response of the output noise is shown in Figure 16. The frequency response of the output voltage

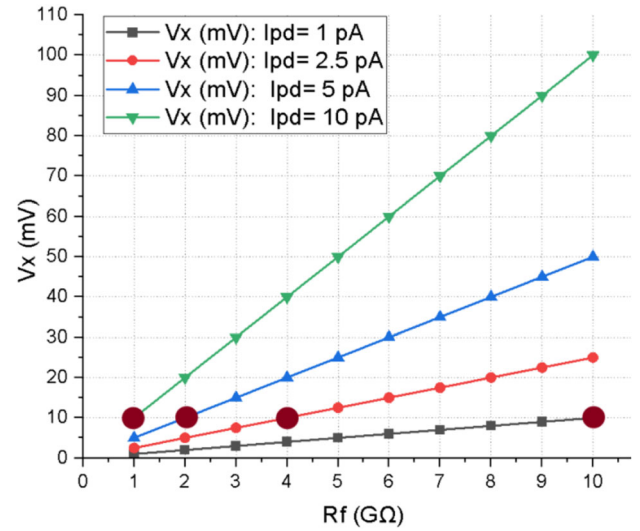


Figure 11. Feedback Resistor vs Output Voltage V_x .

noise of the proposed TIA was observed from 10 Hz–100 MHz. At 10 Hz, the output voltage noise is $40 \text{ pV}/\sqrt{\text{Hz}}$. As the frequency increases, the output voltage noise decreases. The output voltage noise is inversely proportional to the frequency. From the 100 Hz to 10 kHz frequency bands, the noise amplitude was approximately $13 \text{ pV}/\sqrt{\text{Hz}}$. The output noise of the proposed TIA was approximately $1 \text{ pV}/\sqrt{\text{Hz}}$. From noise analysis, it is evident that the output voltage of the proposed TIA exhibits better noise immunity. The output noise of the proposed TIA was calculated using Equation (14).

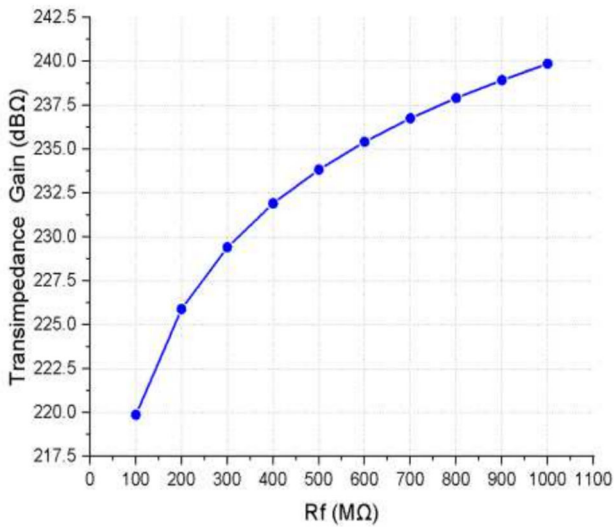


Figure 12. Feedback Resistor vs Transimpedance Gain.

$$V_{n,out}^2 = 4K_B T \times BW \times R_f \quad (14)$$

where,

R_f – Feedback Resistor (GΩ)

The power consumption depends on the operating temperature when all the other parameters are fixed. The effect of temperature on power consumption was observed by changing the operating temperature from -40°C to $+125^\circ\text{C}$, which is the industry-standard range of temperature. When the temperature is -40°C the power consumption is $51.64\ \mu\text{W}$. When the operating temperature was 27°C , that is, room temperature, the power consumption was $115.31\ \mu\text{W}$. When the operating temperature reached 125°C , the power consumption was $324.21\ \mu\text{W}$. From the analysis, it is

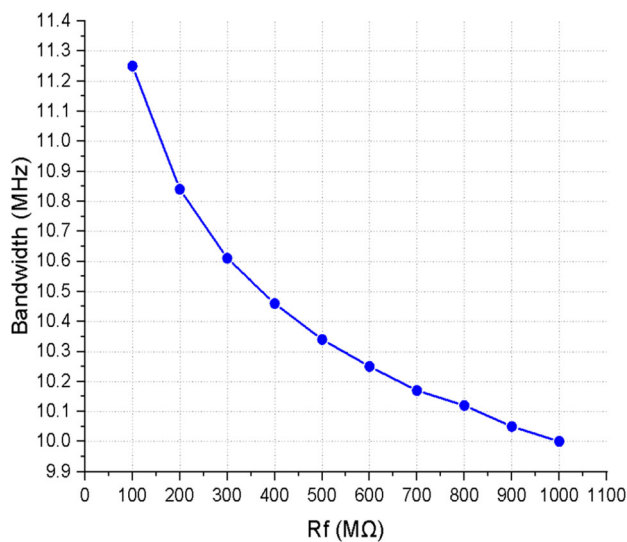


Figure 13. Feedback resistor R_f and the corresponding BW.

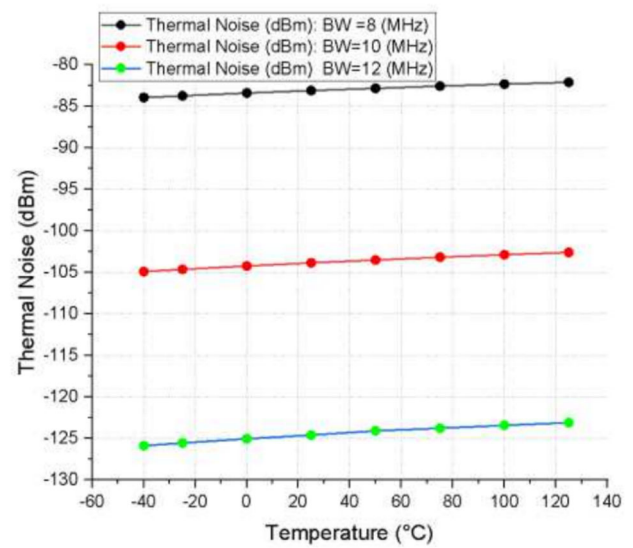


Figure 14. Impact of temperature on the thermal noise.

evident that power consumption increases exponentially with an increase in the operating temperature. Hence, it is necessary to operate the circuit at the minimum possible operating temperature to minimize the power consumption. The impact of temperature on the power consumption is shown in Figure 17. A linear increase in temperature causes an exponential increase in power consumption because the threshold voltage of the transistor decreases exponentially with an increase in temperature.

The impact of the power supply variation on the power consumption was observed by varying the supply voltage from 700 mV to 1500 mV while maintaining the operating temperature at 27°C . From the analysis, it was observed that the power consumption increased exponentially as the

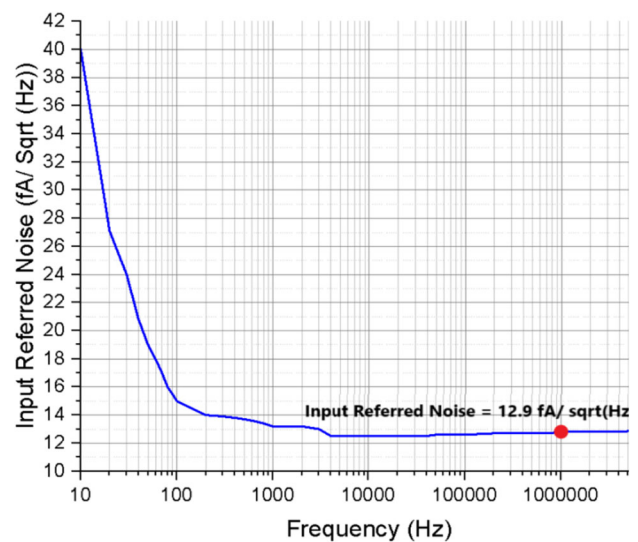


Figure 15. Frequency response of Input referred Noise.

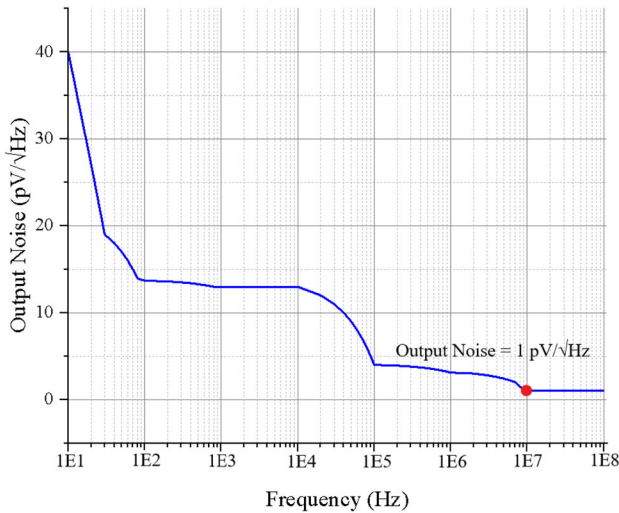


Figure 16. Frequency response of Output Noise.

power supply increased linearly. When the supply voltage was 700 mV, the power consumption was 56.5 μW . When the power supply was 1 V, which is the normal operating voltage, the power consumption was 115.32 μW . When the supply voltage was 50% higher than the normal operating voltage (1.5 V), the power consumption was 259.45 μW . This was 125% higher than the normal power consumption at 1 V. Hence, it is evident that power consumption can be optimized by operating the circuit with the minimum possible supply voltage without affecting the features and functionality of the circuit. Figure 18 depicts the impact of power supply on power consumption. The power consumption of the circuit was directly proportional to V_{dd}^2 .

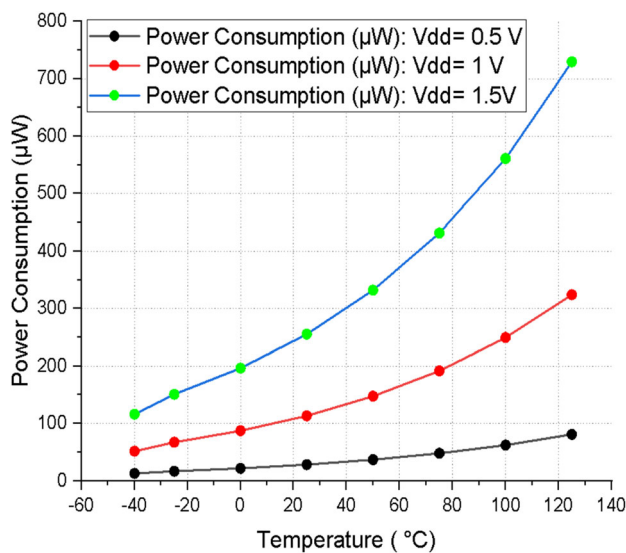


Figure 17. Temperature vs Power Consumption.

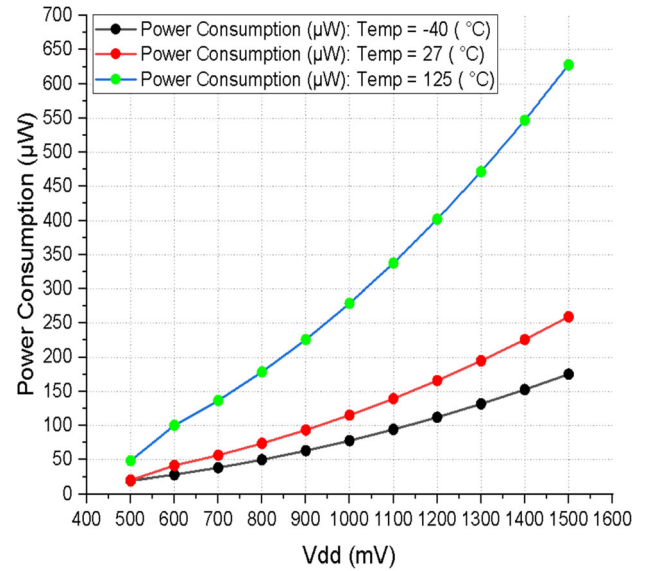


Figure 18. Supply Voltage vs Power Consumption.

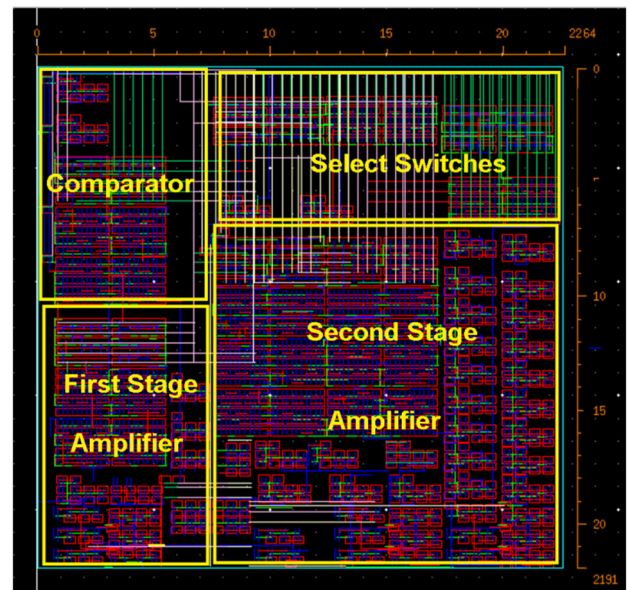


Figure 19. Layout of the proposed Low Input Current TIA.

The layout of the proposed TIA was constructed using the Cadence Virtuoso Layout XL tool. The layout occupied an area of $2264\mu\text{m} \times 2191\mu\text{m}$. The layout of the proposed TIA is shown in Figure 19. Parasitic extraction was performed, and a post-layout simulation was performed to compare the pre- and post-layout results. Good layout-matching techniques were used to minimize parasitic capacitors. However, owing to the large number of load transistors, parasitic capacitors cannot be eliminated. From the comparison, it is evident that the parasitic capacitance from the layout after the back annotation causes a minor

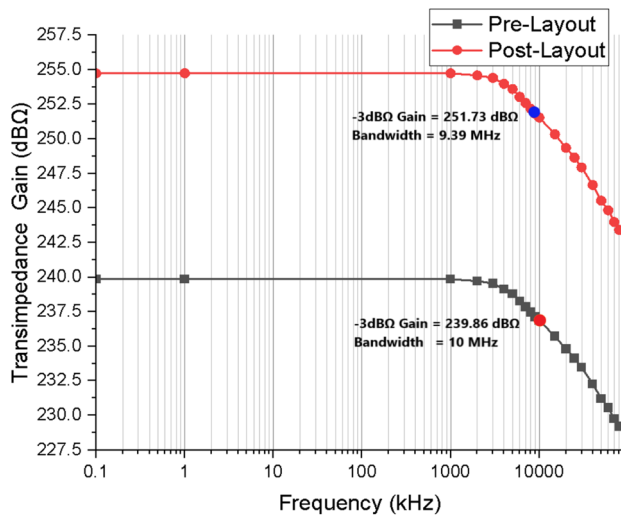


Figure 20. Pre-Layout and Post-Layout Results of the proposed Low Input Current TIA.

shift of approximately 6.2% in the gain and bandwidth of the proposed TIA. The bandwidth was decreased by 6.2%, and the trans-impedance gain was increased to 6.2% from the actual value by maintaining the gain bandwidth (GBW) as a constant.

The frequency response of the transimpedance gain was plotted for the pre-layout and post-layout simulation criteria. The pre- and post-layout simulation results are

presented in Figure 20. From the graph, it is evident that the trans-impedance gain is 239.86 dBΩ and the bandwidth is 10 MHz. In the post-layout simulation, the trans-impedance gain increased by 6.2%, whereas the same amount decreased the bandwidth. From the post-layout simulation, it is inferred that the trans-impedance gain is 254.73 dBΩ and the bandwidth is 9.38 MHz.

The small difference between the schematic simulation and the post-layout is due to a small mismatch in the layout because more transistors are stacked in a cascode manner in the differential pair. This caused a small mismatch in the layout. Owing to the small mismatch, parasitic resistors and capacitors are added to the load capacitor, which shows a difference in the post-layout simulations. However, the variations in the gain and bandwidth can be adjusted to the required values by varying the load capacitor with a trimming capacitor array connected in parallel to the load capacitor and the I_{2bias} current to achieve the required transimpedance gain and bandwidth.

The performance metrics of the proposed low-input-current trans-impedance amplifier are compared with those of other existing TIAs for NIRS biomedical applications in table 6. The proposed TIA was implemented using 45 nm CMOS technology, whereas other TIAs were implemented using 130 & 180 nm technologies. This TIA supports an ultra-low input current of 1pA–10 pA, which is the lowest reported in the literature. This TIA exhibited a trans-impedance gain of 239.86 dBΩ and 10 MHz bandwidth. The supply voltage and power consumption are minimal

Table 6. Performance Comparison.

Description	[10] 2022	[13] 2022	[15] 2022	[19] 2022	[21] 2023	[38] 2024	Proposed Work
Technology (nm)	180	180	180	180	130	180	45
Input Current (peak-peak)	2 nA	64 μA	NA	1 nA	100 nA	1 nA	10 pA
TIG (dBΩ)	123	102	206	124	160	83.5	239.86
Bandwidth	500 KHz	17.5 MHz	3 KHz	555 KHz	10 KHz	98 MHz	10 MHz
Input Noise Current	NA	1.31 (pA/√Hz)	2.69 (fA/√Hz)	390 (fA/√Hz)	1.8 (pA/√Hz)	2.1 (pA/√Hz)	12.9 (fA/√Hz)
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.3	1.8	1
Power	54.2 (μW)	800 (μW)	643 (μW)	36.1 (μW)	400 (μW)	1.1 (mW)	115.31 (μW)
Figure of Merit (FoM)	2800	2750	-	-	-	4065	2078
Topology	CMOS Integrated SOC	Inverter based TIA	Switched capacitor TIA	Tunable Pre-amplifier based TIA	chopper amplifier-based Biosensor	Single-ended TIA	Modified Telescopic CascodeTIA
Applications	Opto-electronic sensing system	Ultrasound Transducer Arrays	Bio-medical devices	Opto-electronic Biomedical Applications		Optical Signal Acquisition	Bio-medical Wearable healthcare devices

compared to those of other TIAs. From the comparative analysis, it is evident that the proposed TIA exhibits outstanding performance in terms of low input current detection in terms of a few picoamperes, high trans-impedance gain and tunability, sufficient bandwidth, low input-referred noise, low output noise voltage, low power consumption, and a better Figure of Merit.

4. Conclusion

A trans-impedance amplifier with ultra-low input current sensing for near-infrared spectroscopic wearable healthcare devices, such as non-invasive glucometers and pulse oximeters, was proposed and implemented in this study. The proposed TIA was implemented using two stages of amplifiers to achieve a maximum transimpedance gain of 239.86 dB Ω and a bandwidth of 10 MHz. A novel variable trans-impedance gain control circuit and saturation mitigation circuit were implemented. The proposed TIA was able to detect and amplify ultra-low-input current in the range of 1pA–10pA. The input referred noise of the proposed is TIA 12.9 fA/sqrt (Hz), and the Figure of merit (FoM) is 2078. This TIA consumes 115.31 μ W of power at room temperature from a 1V power supply. The layout occupied an area of 2264 $\times$ 2191 μ m. The proposed ultra-low input current TIA outperforms the existing TIAs in the literature.

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Data Availability

Complete data are available in this research paper.

Declarations

Conflicts of interest The authors declare no conflict of interest.

Informed Consent Not applicable.

Institutional Review Board Not applicable.

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