



## Voltage Follower, Part II

Welcome to the 34th article in the “Circuit Intuitions” column series. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback as well as your requests and suggestions for future articles in this series. Please e-mail me your comments at ali@ece.utoronto.ca.

In the previous article [1] in this series, we reviewed the general characteristics of a simple voltage follower (SVF) and compared them against those of an ideal voltage follower. An SVF, as shown in Figure 1(a), exhibits an infinite input resistance; a small output resistance, in the order of 1 k $\Omega$ ; and a voltage gain slightly lower than 1 V/V. These characteristics are generally acceptable for a voltage follower except for when the load impedance is in the order of 1 k $\Omega$  or less, reducing the output voltage to less than half of the input voltage. In this article, we review a voltage follower known as a *flipped voltage follower (FVF)* [2], [3] that reduces the output resistance while maintaining the same voltage gain as that of an SVF.

Figure 1(b) shows a schematic of an FVF [2], [3], which consists of two NMOS transistors, M1 and M2. The input voltage is applied to the gate of M1, and the output voltage is

taken from the source of M1, similar to the case of an SVF. The difference between the two circuits lies in the addition of M2 with its gate connected to the drain of M1. Also, the biasing current, which is fed to the source of M1 in the SVF, is now fed to the drain of M1 in the FVF. In fact, moving the current source from the source to the drain of M1 is referred to as *flipping*, and hence the name FVF. Let us now see the characteristics of this voltage follower.

The low-frequency small-signal voltage gain of the FVF is equal to the product of its short circuit transconductance ( $G_m$ ) and its out-

put resistance ( $R_{out}$ ). Figure 2(a) shows a reduced schematic of FVF to determine its  $G_m$  where we have zeroed the ideal dc current source and shorted the output node to ground. This schematic is redrawn in Figure 2(b) to show how the FVF with the shorted output node can be considered as a two-stage amplifier, where the first stage (M1) is a voltage amplifier, and the second stage (M2) is a transconductance. We can write

$$V_{g2} = V_{d1} = -g_m r_o V_{in}$$

where  $g_m$  and  $r_o$  are the transistors' transconductance and the output resistance, respectively. This voltage,

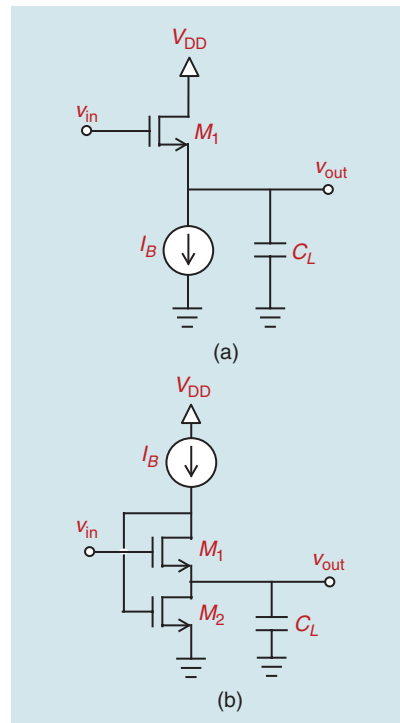


**FIGURE 1:** A schematic of (a) an SVF, also known as a *source follower*, and (b) an FVF.

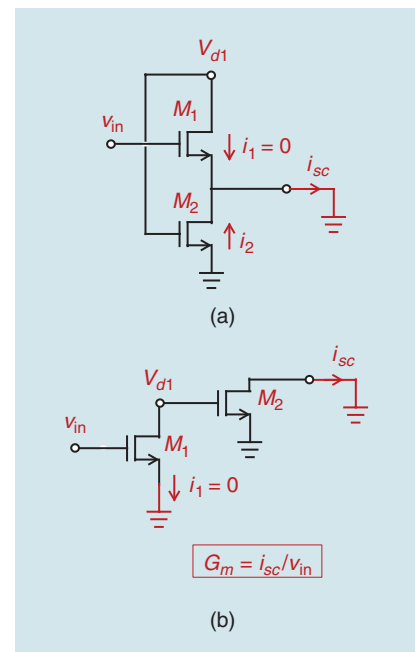


**FIGURE 2:** (a) A small-signal equivalent circuit for the FVF to calculate its transconductance. (b) A redrawn schematic of part (a).

in turn, creates a short circuit current at the output, given by

$$i_{sc} = (g_m r_o) g_m v_{in}$$

where we have assumed both transistors to have the same  $g_m$  and the same  $r_o$ . We can now write

$$G_m = \frac{i_{sc}}{v_{in}} = (g_m r_o) g_m.$$

This equation tells us that the short circuit transconductance of the FVF is  $g_m r_o$  times that of the SVF. Interestingly, this improvement in transconductance is provided by the intrinsic voltage gain of M1 in conjunction with the transconductance of M2. In other words, unlike the SVF circuit in which M1 produces and delivers a small-signal

current to the load, M1 in FVF contributes zero current to the load. The role of M1 in the FVF circuit is to simply amplify the input voltage by  $g_m r_o$  and feed it to the gate of M2. In the FVF circuit, it is M2 (not M1) that produces and delivers the small-signal current to the load. This, in fact, justifies why we can redraw the schematic of Figure 2(a) as shown in Figure 2(b).

Let us now determine the output resistance of the FVF with the aid of Figure 3. Again, we assume that the biasing current source is ideal and remove it for our small-signal analysis. To find the output resistance, we have zeroed the input voltage and applied instead a small-signal test voltage source,  $v_x$ , to the output node. Our goal is now to find the resulting small-signal current that flows into the circuit. This current is the sum of two currents: one that flows through the source of M1 and one that flows through the drain of M2. It is easy to see by inspection that the current through the source of M1 is zero simply because this path will end in an open circuit at the gate of M2. To find the current through M2, we first find the voltage at the gate of M2. Figure 2(b) shows how this can be done easily using a technique described in the first article in this series [4]. We simply find its short circuit current and multiply it by its output resistance. In other words, we can write

$$i_{sc} = v_x \left( g_m + \frac{1}{r_o} \right)$$

where  $g_{me} = g_m + g_{mb}$  is the effective short circuit transconductance of the transistor, including the body effect. Note that the sum of the two terms inside the brackets is the conductance we see looking into the source when the gate and drain are grounded [4].

The output resistance looking at  $v_{d1}$  while the source is grounded is simply  $r_o$ . We can therefore write

$$v_{d1} = i_{sc} r_o = v_x (1 + g_m r_o).$$

This equation tells us that the voltage at the source of a common-gate transistor ( $v_x$ ) is amplified by  $(1 + g_m r_o)$  to arrive at its drain, assuming that the drain is open circuit. This amplified voltage now drives the gate of M2 to produce  $i_2$

$$i_2 = v_x g_m (1 + g_m r_o) + \frac{v_x}{r_o}$$

If we assume that  $g_m r_o \gg 1$ , only the first term in  $i_2$  will be dominant. Hence, we can write

$$R_{out} = \frac{v_x}{i_2} \approx \left( \frac{1}{g_m r_o} \right) \left( \frac{1}{g_m} \right).$$

We found in [1] that the output resistance of an SVF is  $1/g_{me}$ . Therefore, the output resistance of the FVF is a factor of  $1/g_m r_o$  smaller than that of an SVF. This makes intuitive sense because when we apply a small-signal voltage to the output node of an FVF while the input is grounded, the small-signal voltage is amplified and shows up at the gate of M2, effectively increasing its transconductance,

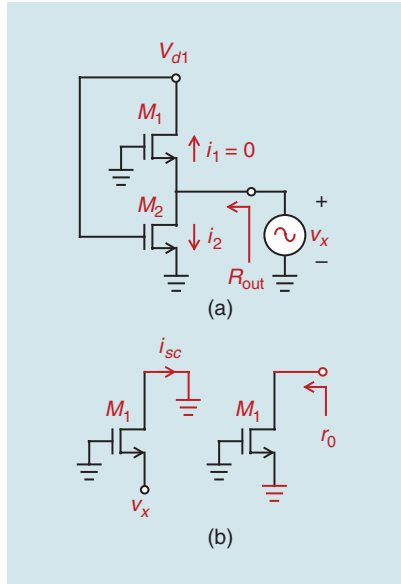


**FIGURE 3:** (a) An equivalent circuit to find the output resistance of an FVF. (b) Equivalent circuits to calculate the gate voltage of M2.

| TABLE 1. NMOS TRANSISTOR PARAMETERS USED IN SIMULATIONS OF THE SVF AND FVF. |                  |
|-----------------------------------------------------------------------------|------------------|
| PARAMETER                                                                   | NMOS (M1 & M2)   |
| W/L                                                                         | 400 nm/45 nm     |
| $ V_T $                                                                     | 0.43 V           |
| $g_m$                                                                       | 0.5 mS           |
| $g_{mb}$                                                                    | 0.15 mS          |
| $r_o$                                                                       | 11.15 k $\Omega$ |

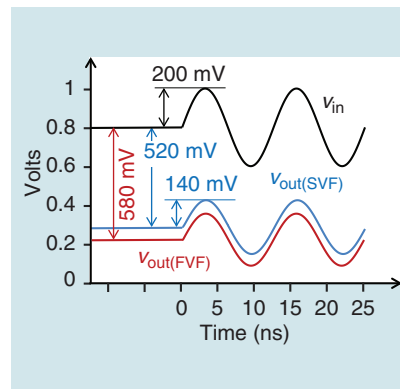


**FIGURE 4:** A pair of input voltage waveform (in black) and output voltage waveforms of (a) an NMOS SVF (in blue) and (b) an NMOS FVF (in red).

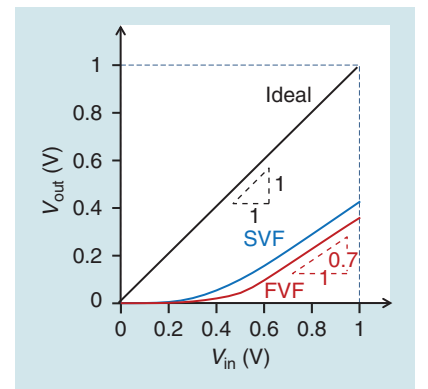


**FIGURE 5:** The simulated dc behavior of an NMOS SVF (in blue) and NMOS FVF (in red) compared to that of an ideal voltage follower (in black).

pulling a larger current from the applied voltage source; that is, it exhibits a much smaller resistance.

Another intuition for smaller output resistance can be provided with the help of negative feedback. If the output voltage increases for any reason (say from an increase in the load resistance), it will reduce the  $v_{gs}$  of M1 and, in turn, the current that M1 feeds to the output node, lowering the output voltage. This negative feedback effectively “resists” a changing output voltage or, equivalently, provides a low output resistance.

We now multiply the expressions for  $G_m$  and  $R_{out}$  to determine the voltage gain of the FVF

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m}{g_{me}}.$$

Interestingly, this voltage gain is identical to what we have found [1] for the voltage gain of an SVF. However, we note that in the case of an FVF, this same voltage gain is obtained by the product of a much higher transconductance (by a factor of  $g_m r_o$ ) and a much lower output resistance (by a factor of  $1/g_m r_o$ ). This is interesting as it shows how the FVF achieves our final goal of having a voltage gain of around one while reducing the output resistance substantially.

We have used the parameters shown in Table 1 with a nominal bias current of  $I_B = 50 \mu A$  and a load capacitance of  $C_L = 100$  fF to simulate both the SVF and the FVF circuits and to compare their dc characteristics and frequency responses. Figure 4 shows that, for the parameters used, both SVF and FVF shift down the input voltage waveform by around the same dc value, although with a slightly higher shift in the case of the FVF: 580 mV for the FVF versus 520 mV for the SVF. This larger shift in the FVF is due to a small voltage drop across a nonideal current source we have used in our simulations. This voltage drop effectively reduces  $V_{DS1}$  in the FVF, causing a larger  $V_{GS1}$  to accommodate the same nominal current through M1. Finally,

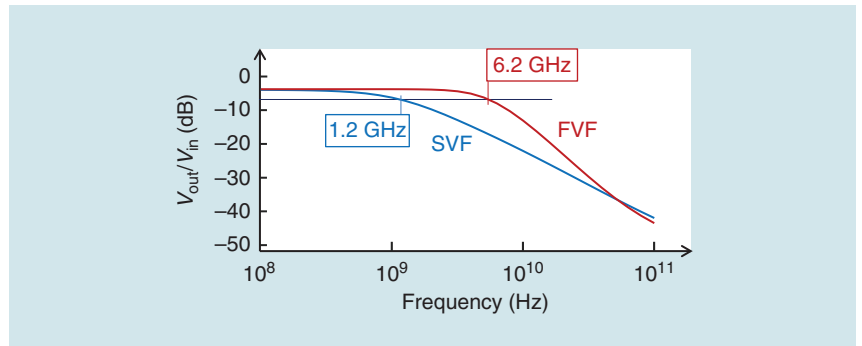


**FIGURE 6:** Voltage gains of FVF (in red) and SVF (in blue) as functions of frequency.

note that both designs exhibit a similar voltage gain of  $g_m/g_{me}$ , which is around 0.7 V/V.

Figure 5 compares the dc characteristics of the two followers against that of an ideal voltage follower. We observe that the outputs of the SVF and the FVF follow their respective input only for input voltages larger than about 0.6 V. For this range, any voltage increment at the input appears as a voltage increment at the output albeit with a factor of around 0.7 V/V.

Finally, given a reduction in the output resistance of the FVF compared to that of the SVF, by a factor of  $g_m r_o$ , we expect the FVF to have an increased bandwidth by the same factor. This is indeed consistent with the simulation results shown in Figure 6 where the FVF bandwidth of ~6.2 GHz is five times the SVF bandwidth of ~1.2 GHz. The simulation results of Figure 6 further reveal a 40-dB/dec drop in the voltage gain of the FVF, compared to a 20-dB/dec drop for the SVF. The readers are encouraged to explain why this is the case before reading further.

A short answer is that the signal path from the input to output of the SVF has a single pole, corresponding to the output node, assuming that we drive the input node with an ideal voltage source. In contrast, the signal path of the FVF has two poles: one at the output node and one at the gate of M2. To see this intuitively,

one should note that the voltage transfer function of the FVF is a product of its short circuit transadmittance (having a pole at the gate of M2) and its output impedance (having a pole at the output node).

In summary, we have shown that an FVF offers the same voltage gain as that of an SVF; however, it does so by providing a much larger short circuit transconductance and much lower output resistance. There are further variations and improvements that can be made to the FVF circuit, and we will cover some of them in Part 3 of this series.

## Acknowledgment

Many thanks to Jeremy Cosson-Martin for his assistance with the simulation results in this article.

## References

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