

A 800MHz–3.8GHz 1.6-dB NF Inductorless Wideband CMOS LNA for Wireless Communications

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Abstract- In this paper, we present a inductorless, wide-band, low-noise balun amplifier (LNA) for multistandard applications. The LNA adopts a complementary current-reuse common source(CS) amplifier, combined with a low-current active feedback to achieve high voltage-gain and wideband input matching. In addition, The LNA employs a common gate(CG) - common source load to achieve differential output. This solve the problem of the trade-off between low noise and high linearity in the circuit. Our LNA has higher gain and lower NF compared with the conventional CS- active feedback LNA. By 65-nm RF CMOS process, the LNA can achieve a voltage gain of 26 dB, a IIP3 of -6.6 dBm at 2.4 GHz and an NF of 1.6–1.8 dB over a 3-dB bandwidth of 0.8–3.8GHz in theory. It consumes 4.4 mA from a 1.2-V supply and occupies an active area as compact as 0.046 mm².

Index terms- CMOS, inductorless, low power, low noise amplifier, multi-standard, broadband.

I. INTRODUCTION

Nowdays mobile communication standards have advanced from the first to the fifth generation cellular mobile communication technology (5G) with wider bandwidths and higher transmission rates [1], [2]. In addition, Wi-Fi (IEEE 802.11b/1/g/n/ac/ax) and Bluetooth standards also hold significant positions. Current devices are capable of supporting over 10 standards and covering more than 30 frequency bands. Instead of multiple fixed narrowband radio frequency (RF) receivers using multiple chip designs [3] which have drawbacks such as high cost, accumulated total power, and limited flexibility, a single broadband LNA compatible with multiple communication standards become a better choice.

As the primary active component in the first stage, LNA plays a key role in above system. Its design specifications include input matching, noise figure, and linearity within the operating frequency range. For RF receiver, single-ended LNAs are preferred, because antenna and off-chip filtering ports are typically single-ended. Its direct transmission avoids off-chip balun at the input, resulting in reduced chip area and insertion loss [4], [5].

Recent broadband, inductorless low-noise amplifiers (LNAs) can be classified into three types include CS amplifiers with resistive [6] or active feedback [7]-[9], CG amplifiers

incorporating gain [10] or noise-canceling techniques [11], and CG-CS LNAs based on noise-canceling structures [12]-[15]. However, these designs suffer from significant trade-offs between gain and matching and supply voltage and noise figure.

As an improvement, this paper introduces an innovative broadband, inductorless LNA designed for low-power applications. It simultaneously supports over 7 different communication standards: WCDMA, E-GSM, DCS, PCS, WLAN, Bluetooth, and LTE (low-frequency bands). Table I summarizes the specifications such as voltage gain, noise figure (NF), and linearity (IIP3) for each standard [16], [17].

These metrics are targeted for the worst-case scenario of the wireless link, i.e., maximum sensitivity and high linearity. If not all specifications need to be met or if wireless link conditions improve, power consumption can be saved.

II. INDUCTORLESS LNA DESIGN

As shown in Fig. 1, the proposed LNA combines active feedback principles with a transmission impedance amplifier and integrates a Balun structure into the CS active feedback LNA. This configuration enables the transformation of single-ended input to differential output, thereby improving system linearity. In addition a PMOS transistor is connected to the input terminal of MN1, utilizing current-reuse techniques to enhance the circuit's equivalent transconductance.

TABLE I

LNA REQUIREMENTS BY WIRELESS STANDARDS

Frequency Standard	Band (MHz)		Requirement		
	Low	High	Gain (dB)	NF (dB)	IIP3 (dB)
E-GSM	880	960	18	3	-5
DCS	1710	1800	18	3	-5
PCS	1850	1990	18	3	-5
Bluetooth	2400	2480	18	5	-5
WLAN	2400	2483	18	3	-5
LTE	700	3800	18	5	-10
WCDMA	1920	2170	18	2	0

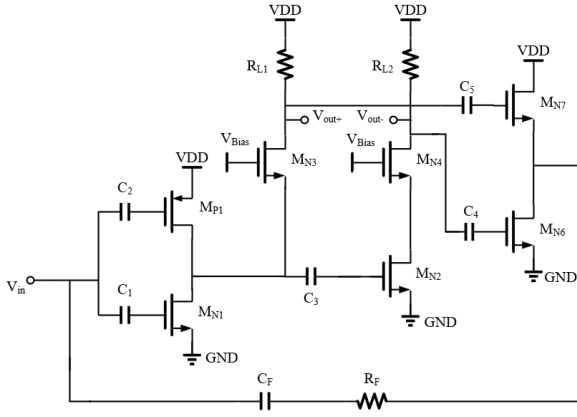


Figure 1. Proposed LNA implementation.

1) *Voltage Gain*: the voltage gain of the reverse and forward signal path is calculated by:

$$A_{V1} = -G_{m1} \cdot R_{L1} \quad (1)$$

$$A_{V2} = G_{m1} \cdot \frac{g_{mn2} \cdot R_{L2}}{g_{mn3}} \quad (2)$$

The gain balance is achieved when

$$G_{m1} \cdot R_{L1} = G_{m1} \cdot \frac{g_{mn2} \cdot R_{L2}}{g_{mn3}} \quad (3)$$

2) *Input Impedance Matching*: The resistance and impedance of the feedback circuit and the voltage generator are synthesized to the input of the amplifier circuit using Miller's theorem, which can be expressed as

$$Z_1 = \frac{R_F + \frac{1}{g_{mn7}}}{1 + 2(g_{mn1} + g_{mp1})R_{L1,2}} \quad (4)$$

The equivalent impedance of the input MOS transistor and the bond wire inductance L_s is:

$$Z_2 = \frac{1}{sC_{gs,mn1}} + sL_s + \frac{g_{mnl}(L_s)}{C_{gs,mn1}} \quad (5)$$

Therefore, the input impedance can be obtained as:

$$Z_{in} = sL_1 + Z_1 \left\| \left(\frac{1}{sC_1} + Z_2 \right) \right\| \left(\frac{1}{sC_2} + Z_3 \right) \quad (6)$$

3) *Noise Factor*: The noise factor under input impedance matching condition can be expressed as

$$F \approx 1 + \frac{v_{Mnx(x=1,2,6,7)}^2 + v_{Mpl}^2 + v_{RF}^2 + v_{RL1}^2 + v_{RL2}^2}{v_{RS}^2} \quad (7)$$

$$\approx 1 + EF_{Mnx(x=1,2,6,7)} + EF_{Mpl} + EF_{RF} + EF_{RL1} + EF_{RL2}$$

where EF is the excess noise factor to quantify the contribution of different devices to the overall noise factor F .

$$EF_{Mn1} \approx \frac{4kT\gamma g_{d0} \cdot R_{L1}^2}{4kTR_s \cdot [(g_{mn1} + g_{mpl})R_{L1}]^2} \approx \frac{\gamma}{\alpha} \cdot \frac{1}{R_s} \cdot \frac{g_{mnl}}{(g_{mn1} + g_{mpl})^2} \quad (8)$$

$$EF_{Mpl} \approx \frac{4kT\gamma g_{d0} \cdot R_{L2}^2}{4kTR_s \cdot [(g_{mn1} + g_{mpl})R_{L2}]^2} \approx \frac{\gamma}{\alpha} \cdot \frac{1}{R_s} \cdot \frac{g_{mpl}}{(g_{mn1} + g_{mpl})^2} \quad (9)$$

$$EF_{Mn2} \approx \frac{\left(\frac{1}{2}\right)^2 4kT\gamma g_{d0} \cdot R_{L1,2}^2}{4kTR_s \cdot [(g_{mnl} + g_{mpl})R_{L1,2}]^2} \quad (10)$$

$$\approx \frac{1}{4} \cdot \frac{\gamma}{\alpha} \cdot \frac{1}{(g_{mnl} + g_{mpl})R_s} \cdot \frac{g_{mn2}}{(g_{mnl} + g_{mpl})}$$

$$EF_{RL1,2} \approx \frac{\left(\frac{1}{2}\right)^2 \cdot 4kTR_{L1,2}}{4kTR_s \cdot [(g_{mnl} + g_{mpl})R_{L1,2}]^2} \approx \frac{1}{4} \cdot \frac{1}{(g_{mnl} + g_{mpl})^2 R_{L1,2} R_s} \quad (11)$$

Equivalent noise contributions from each component in the feedback path are calculated respectively at the input terminal:

$$EF_{RF} \approx \frac{R_s}{R_F} \cdot \left(\frac{\frac{R_F}{1 + R_F + R_s}}{g_{mnx}} \right)^2 \approx \frac{R_s}{R_F} \quad (12)$$

$$EF_{Mnx(x=6,7)} \approx \frac{\gamma}{\alpha} \cdot \frac{g_{mnx} R_s}{[1 + g_{mnx} (R_F + R_s)]^2} \quad (13)$$

III. SIMULATION RESULTS

The low-noise amplifier (LNA) can be implemented by TSMC 65nm CMOS process. The circuit draws 4.4mA of current from a 1.2V power supply. The circuit was designed using the Cadence design environment and simulated using Spectre-RF. Fig. 2 shows the post-simulation results of S11. Across all process corners, S11 remains <-10dB in 0.8-3.8GHz. It proves the proposed technique delivers broadband input matching. As depicted in Fig. 3, the voltage gain peaks at 26.8dB at a frequency of 2.3GHz and maintains a 1dB flatness within 800MHz-3.8GHz. Therefore, the LNA can significantly mitigate the noise contribution of subsequent stages.

The NF of the LNA, as given in Fig. 4, is 1.6dB at a frequency of 2.45GHz, with the NF<1.8dB in entire frequency range. A two-tone measurement of intermodulation distortion

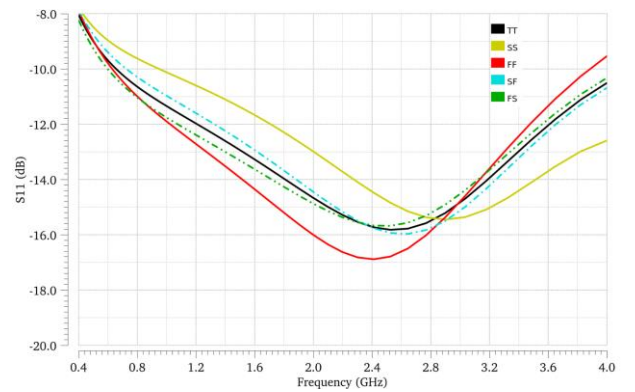


Figure 2. Input impedance variation with process corners.

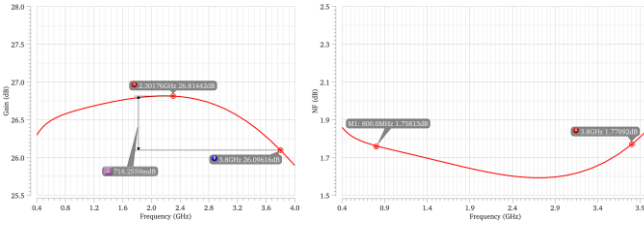


Figure 3. Simulated voltage gain of the proposed LNA.

Figure 4. Simulated NF of the proposed LNA.

was carried out at various frequencies (f_0) with different spacings (Δf). Fig. 5 shows the IIP_3 at $f_0 = 2.4$ GHz and $\Delta f = 1$ MHz. Fig. 6 depicts the IIP_3 from 800 MHz to 3.6 GHz with $\Delta f = 1$ MHz and 50 MHz. The circuit layout is shown in Fig. 7, with the area of LNA core less than 0.046 mm^2 .

The variation of the other performance parameters, relative to the typical corner, are shown in Fig. 8. As observed from it, the process variations have a minor impact on LNA performance with the values, all within 10%.

The performance of the LNA is summarized in Table II and compared with that in previous published works. The proposed circuit exhibits high linearity while consuming minimal power. This LNA covers most wireless standards, including 4G and 5G, in the range of 0.8–3.8 GHz.

IV. CONCLUSION

In this paper, a wideband noise-cancelling LNA without the use of on- or off-chip inductors has been designed for low-voltage low-power applications. The proposed topology is applicable for highly integrated multi-standard radio receivers.

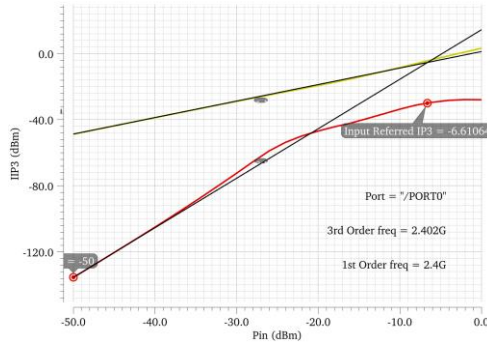


Figure 5. Simulated IIP_3 of the proposed LNA.

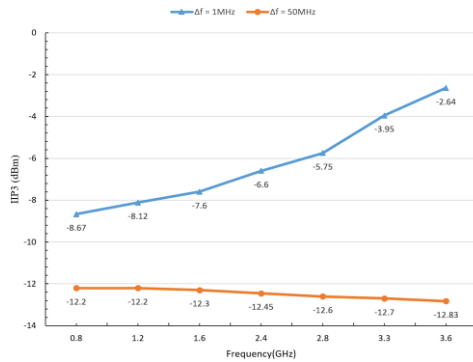


Figure 6. IIP_3 versus frequency for different tone spacings.

It takes advantage of current-reuse technique to achieve both high gain and low power consumption. Due to the differential output obtained by CG-CS load employed, trade-off between low noise and high linearity has been addressed. With 65-nm RF CMOS process, the LNA achieves a voltage gain of 26 dB and an NF of 1.6–1.8 dB over a 3-dB bandwidth of 0.8–3.8GHz. It consumes 4.4 mA from a 1.2-V supply and occupies an active area of only 0.046 mm^2 . Benefiting from the technique introduced in this paper, our LNA provides comparable and even better NF and gain than those of reported inductorless LNAs at even lower power consumption and lower supply voltage.

ACKNOWLEDGMENT

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Due to page limit, references are omitted here. please contact the author for the detailed list if it is needed.

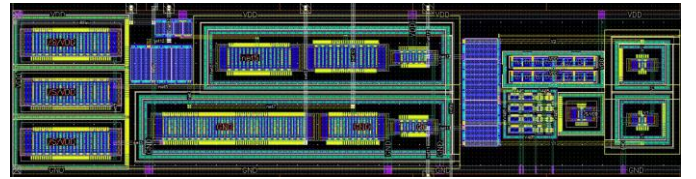


Figure 7. Layout diagram of LNA.

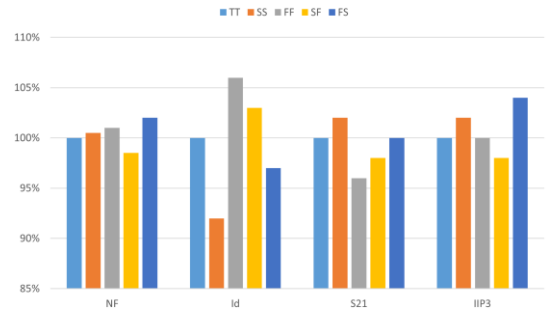


Figure 8. Performance variation relative to typical corner (TT) at 2.4 GHz.

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED
WIDEBAND LNAs

Ref	Process	Topology	Frequency (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)
[7]	90nm	Active FB	0-6	<-10	17.4 ^{PG}	2.5	-10	1.2	9.8
[8]	130nm	Active FB	0.1-5	<-10	18-20	2.5-4	-8	1.2	20
[9]	65nm	Active FB	0.7-2.2	<-10	21.9-26.8	2.9-3.8	-13	1.2	10.8
[10]	180nm	CC-CG	3.1-10.7	<-10	8.5	4.4	7.4	1.8	4.5
[11]	0.5μm	CC-CG	0.8-0.95	<-10	12.2	3	6.7	2.7	27
[12]	65nm	CG-CS	0.2-5.2	<-10	13-15.6	2.9-3.5	0	1.2	21
[13]	65nm	CG-CS	0.05-1	<-10	24-30	2.3-3.3	-4.1	2.2	19.8
[14]	65nm	CG-CS	0.5-7	<-10	18	4.5-5.5	-3	1.2	16
[15]	130nm	CG-CS	0.2-3.8	<-9	19	2.8-3.4	-4.2	1	5.7
This work	65nm	Active FB + CG-CS	0.8-3.8	<-10	26	1.6-1.8	-6.6	1.2	5.28