

Asymmetric and Double-Layered Gate-All-Around Structures of 1T-DRAM for Sensing Margin and Retention Improvement

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Abstract—A general dynamic random access memory (DRAM) is consisted of transistor and capacitor and has continuously scaled down the cell size for larger memory density. However, one transistor-DRAM (1T-DRAM) is a promising device, which integrates both transistor and capacitor into one transistor. In this article, 1T-DRAM is a gate-all-around (GAA) structure, and silicon germanium (SiGe) and silicon were used as body and source/drain to form a quantum well in the valence band. The performance of 1T-DRAM is decided with sensing margin and retention. Expanding the capacity of the quantum well and lowering the recombination rate in the body are desired. Therefore, three body structures are proposed to improve the performance of the 1T-DRAM while maintaining its cell size. First, asymmetric structure is proposed to decrease the recombination rate at the underlap region between the body and source by lowering the mole fraction. Since the recombination relieves as the mole fraction decreases, it is possible to improve the retention by lowering the mole fraction. In addition, the double-layered structure is designed to increase the capacity of the quantum well by increasing the mole fraction of the outer layer. Finally, asymmetric double-layered structure is proposed. Since the targets by asymmetric double-layered structure are the retention and the sensing margin, respectively, the integrated structure can improve both performance metrics. The results are verified using the calibrated TCAD modeling and simulations.

Index Terms—Capacitorless, gate-all-around (GAA), one transistor-dynamic random access memory (1T-DRAM), retention, sensing margin, silicon germanium (SiGe).

I. INTRODUCTION

THE most commonly used volatile memory, dynamic random access memory (DRAM) has been widely used in electronic devices since it received attention due to its high-speed operation and integration density [1]. The number of DRAM cells per chip has exponentially increased due to its excellent scalability based on structure simplicity.

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However, DRAM cells have faced problems, such as high leakage current or low cell capacitance, as the scale of the cell is decreased. To overcome these problems, researchers have continuously suggested structures that can relieve the problems and improve DRAM cell performance. It is believed that cell capacitance has increased due to high- k materials and cylindrical capacitor designs [2], [3]. Especially, the cylindrical capacitor has been manufactured with an excessive aspect ratio [4]. Nevertheless, it is difficult to deal with the capacitor due to complex fabrication steps. Therefore, one transistor-DRAM (1T-DRAM) has emerged as the next generation since it acts as a DRAM with only one transistor. It can also take the advantage of cell area by integrating both transistor and capacitor into one transistor. Consequently, it increases the memory density and decreases the cost of fabrication.

There are various structures for 1T-DRAM. Structures, such as silicon-on-insulator, double gate, or gate-all-around (GAA), usually used to accumulate hole carriers in a floating body [5], [6], [7]. GAA structure device has outstanding gate controllability over planar structure and is used in devices, such as NAND flash memory [8]. Furthermore, study about the junctionless (JL) structures is investigated for 1T-DRAM, which is a way to reduce the OFF-current [9]. In this article, modified structures are proposed to enhance the performances of 1T-DRAM in utilizing both GAA and JL structures, which are calibrated using Sentaurus TCAD modeling and simulations. Each modification improves sensing margin and retention by manipulating the energy band of the body without any additional cell area requirement.

II. 1T-DRAM STRUCTURE AND OPERATION

A. 1T-DRAM Structure

1T-DRAM is designed as a JL FET with a GAA structure using as shown in Fig. 1. Here, 1T-DRAM is consisted of source, drain, and body, and it is covered with oxide. The radius of the 1T-DRAM (R) is 10 nm, and the thickness of the oxide (T_{ox}) is 2 nm. The length of the drain and source (L_{ds}) is 50 nm and the lengths of the gate (L_g) and underlap region ($L_{underlap}$) are 70 and 15 nm. The source and drain are n-type silicon (Si), and the body is n-type silicon germanium (SiGe) with a uniform mole fraction.

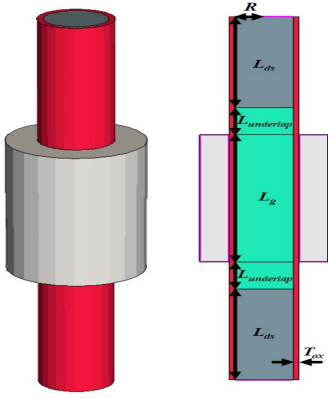


Fig. 1. Structure and vertical cutline of a 1T-DRAM.

TABLE I
PHYSICAL PARAMETERS OF 1T-DRAM

Parameter	Value
L_{ds}	50 nm
L_g	70 nm
$L_{underlap}$	15 nm
R	10 nm
T_{ox}	2 nm
D_{ds}	$5 \times 10^{19} \text{ cm}^{-3}$
D_b	$1 \times 10^{18} \text{ cm}^{-3}$
D_{it}	$1 \times 10^{11} \text{ cm}^{-3}$
E_{it}	0.1 eV

The source and drain are doped with the concentration (D_{ds}) of $5 \times 10^{19} \text{ cm}^{-3}$ and the body is doped with the concentration (D_b) of $1 \times 10^{18} \text{ cm}^{-3}$, which was optimized as the sensing margin and retention are in a tradeoff relation depending on the doping concentration of the body. The mole fraction of the body must also be considered since it decides the quantum well in the body, which determines the electric characteristics, sensing margin, and retention [10]. The oxide is fabricated with the hafnium oxide (HfO_2), which covers the whole device. The gate metal is Mo with a work function of 5.0 eV. Since the work function and dielectric constant of the oxide are high, there is high difference of quasi Fermi level between the body, source, and drain. Consequently, the body creates a quantum well in the valence band, although it is a JL FET. Furthermore, the underlap regions between the body and source and the body and drain are for relieving the severe electric field due to the high difference of quasi Fermi level. Each acceptor like and donor like traps are placed at the interface between the body and gate oxide to consider trap-assisted tunneling [11]. The trap density (D_{it}) is $1 \times 10^{11} \text{ cm}^{-3}$, and the energy difference (E_{it}) with the conduction band (in case of the acceptor like trap) or valence band (in case of the donor like trap) is 0.1 eV. The physical parameters are summarized in Table I.

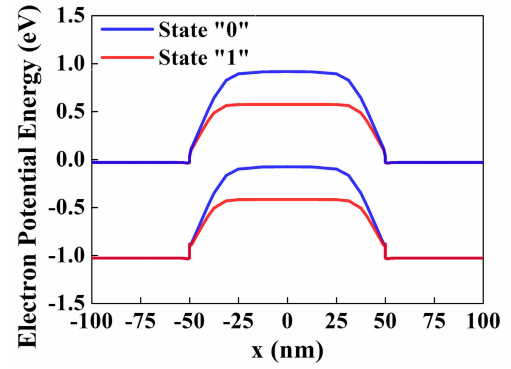


Fig. 2. Energy band of the uniform body 1T-DRAM on each state.

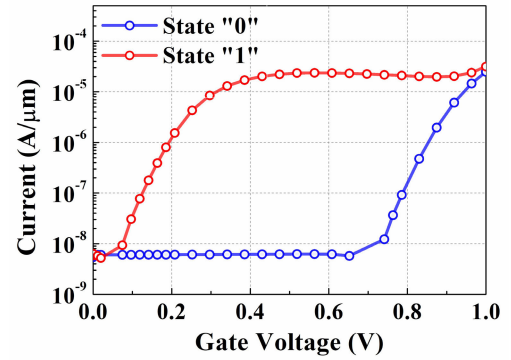


Fig. 3. Transfer curve of uniform body 1T-DRAM at state "1" and "0."

B. Operation and Simulation Setting

The device has two states, which are state "1" and state "0." The state "1" means that the body is filled with hole carriers, and the state "0" means that the body is empty. As shown in Fig. 2, the energy band of the body differs depending on which state it is. In other words, the amount of hole carriers gathered in the body determines the energy band. This is because the hole carriers function as a positive charge given to the body. In the perspective of electron moving from the source to the drain, the energy barrier is different depending on the state, which results in different currents. Fig. 3 shows the transfer curve in different states. Consequently, it is possible to distinguish which state it is by measuring the current when a bias called "read" is given to the drain and gate voltage 10 ns after writing the state. The band-to-band tunneling (BTBT) is the main process to write state "1." It is known that BTBT is used as writing state "1" in 1T-DRAM with narrow bandgap materials [12]. Positive drain voltage and negative gate voltage are given to write state "1." As shown in Fig. 4(a), the bandgap of the underlap region is narrow, so that the BTBT rate increases significantly and the holes generated by BTBT are accumulated in the quantum well. On the other hand, positive gate voltage and negative drain voltage are given to write state "0." As shown in Fig. 4(b), the valence band has a slope toward the drain, so that the hole carriers can escape to the drain. The bias conditions for each operation are summarized in Table II.

A performance of memory is estimated with sensing margin and retention. The sensing margin is the current difference

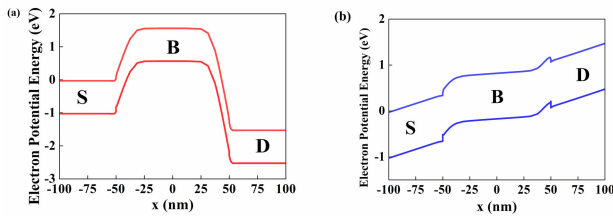


Fig. 4. Energy band of the 1T-DRAM when writing (a) state "1" and (b) state "0."

TABLE II

BIAS CONDITIONS OF EACH OPERATION

Operation	Write "1"	Write "0"	Read	Hold
V_G	-1.0 V	1.0 V	0.7 V	0 V
V_D	1.5 V	-1.5 V	0.1 V	0 V

of the read current at each state. A large quantum well can increase the sensing margin because the hole carrier density gathered in the body leads a higher energy barrier difference of each state. The retention time indicates how long the memory maintains its state. It is defined how long it takes to decrease the sensing margin to 50% compared to the initial sensing margin. Sensing margin was monitored after 10 ns, 1 ms, 10 ms, 64 ms, and 100 ms of hold time, and the retention time was calculated by linearly interpolating the hold time when the sensing margin becomes half. It showed that the calculated retention time of uniform body 1T-DRAM with $\text{Si}_{0.7}\text{Ge}_{0.3}$ was 49 ms, while simulated retention time was 46 ms, which was quite precise. After writing state "1" or state "0," it is difficult to remain its state due to Shockley–Read–Hall (SRH) recombination and trap-assisted-tunneling (TAT) that happens in the body. The mole fraction and doping concentration of the body were optimized considering the sensing margin and retention, since the performance is in tradeoff relation. It is known that higher mole fraction of SiGe increases the offset of the energy band level compared to Si and results in stronger quantum confinement effect [13]. A higher doping concentration of the body increases the energy band level of the body since the body is fully depleted.

To estimate the performance of 1T-DRAM, Sentaurus TCAD simulation tools are used for the calibration [14]. Self-consistent Poisson equation, continuity equation, and density-gradient equation are solved to calculate the potential and drain current in the simulation. Nonlocal BTBT was used, and the coefficients of Kane and Keldysh model, A and B, were interpolated between Si and Ge. SRH recombination, Hurkx TAT, and quantum confinement models were also adapted. The lifetimes of the carriers in Si and SiGe were $\tau_n = 1 \times 10^{-5}$ s and $\tau_p = 3 \times 10^{-6}$ s and $\tau_n = 5 \times 10^{-6}$ s and $\tau_p = 5 \times 10^{-7}$ s [15], [16]. The lifetime was dependent to doping concentration and electric field. The lifetime was dependent on the doping concentration and the electric field. Philips unified and Lombardi mobility models were included to consider the degradation due to impurity scattering and electric field. In this work, Slotboom bandgap narrowing

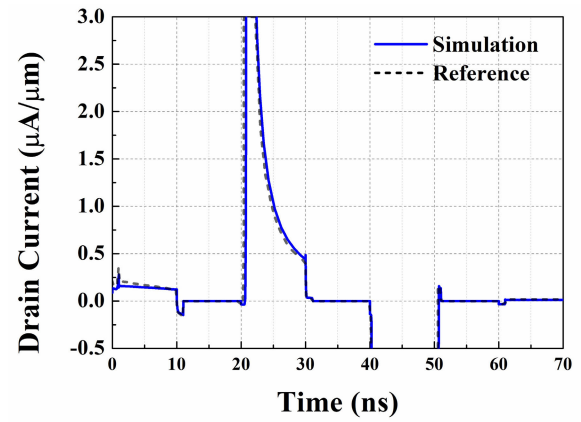


Fig. 5. Calibrating transient simulation of reference for estimating sensing margin of uniform body 1T-DRAM.

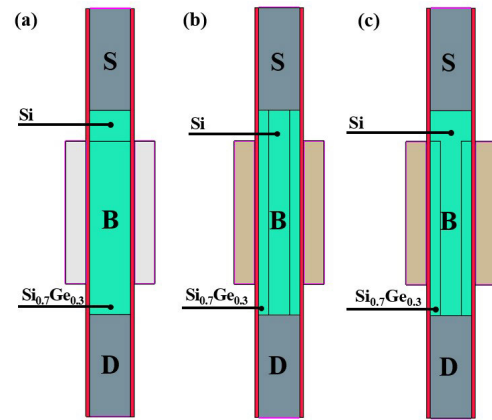


Fig. 6. Vertical cutlines of (a) asymmetric, (b) double-layered, and (c) asymmetric double-layered structures of 1T-DRAM.

model and Fermi Dirac statistics were also used for an accurate calculation since the device was heavily doped.

As a result, it was able to calibrate the transient simulation of previous study of GAA JL FET, which was consisted of $\text{Si}_{0.8}\text{Ge}_{0.2}$ as the body, as shown in Fig. 5 [7]. Moreover, the physical parameters, such as energy bandgap and BTBT parameters, were also applied based on the studies of SiGe [17].

Hole carriers are gathered in writing state "1" and a sudden drain current occurs in reading state "1" after a 10 ns of hold time. The drain current increases rapidly since the threshold voltage is low in state "1" and the gate voltage increases to 0.7 V in the first 1 ns of reading. The drain current decreased after reaching to the bias condition of reading because recombination occurs in the body as both hole and electron carriers are abundant. The threshold voltage rises as the hole carriers gathered in the body decrease.

III. MODELING SCHEMES AND RESULTS

Three body structures were proposed to improve the performances of this basic structure. They are asymmetric, double-layered, and both asymmetric and double-layered structures, as shown in Fig. 6. These proposed structures can be fabricated using the conventional vertical trench processes,

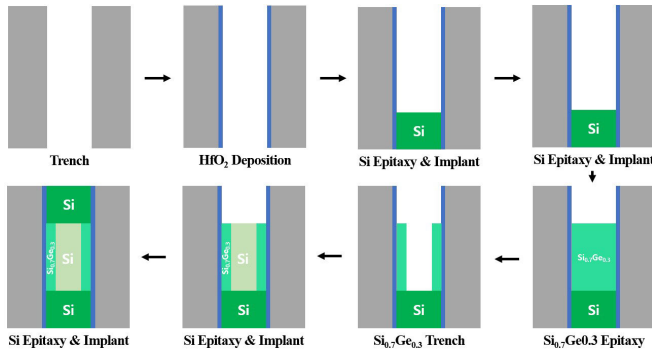


Fig. 7. Process steps to fabricate double-layered structure 1T-DRAM.

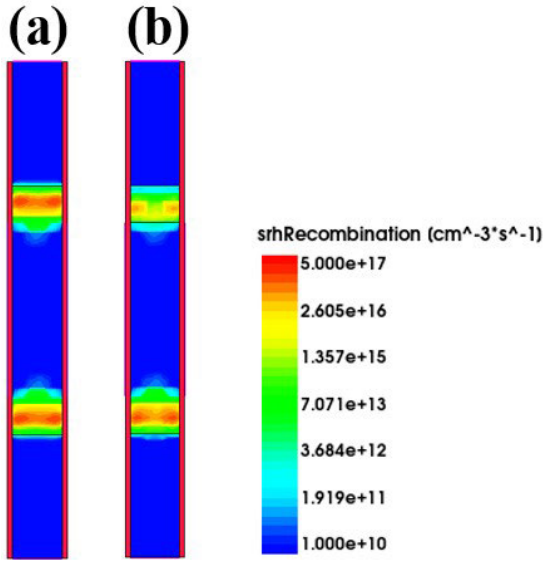


Fig. 8. Recombination rate of (a) uniform body and (b) asymmetric body structure in equilibrium state ($V_G = V_D = V_S = 0$ V).

which are used for V-NAND flash memory fabrication and epitaxy process shown in Fig. 7 [18], [19], [20]. Epitaxy has a risk of defects due to different growth rates in different crystal directions [21], [22]. However, there are recent researches about epitaxy process, such as high level of control epitaxy process for nanowire using metal catalyst with precursor provided in different conditions [23] or silicon substrate patterning to restrict motions of defects [24].

A. Asymmetric Structure

The asymmetric structure was proposed to reduce the recombination rate on the source-side underlap region. The underlap region exists to reduce the recombination rate since a strong internal electric field occurs due to the difference of quasi fermi level between body, source, and drain. However, the drain-side underlap region was dominant in writing state “1” as the BTBT rate on the drain side was 10^5 times higher than the source side. Therefore, it is possible to reduce the recombination rate and increase the retention time with placing Si at the source side underlap region.

As a result, the recombination rate on the source side decreased when $V_G = V_D = V_S = 0$ V, as shown in Fig. 8. The decreased recombination rate brought out an increase in

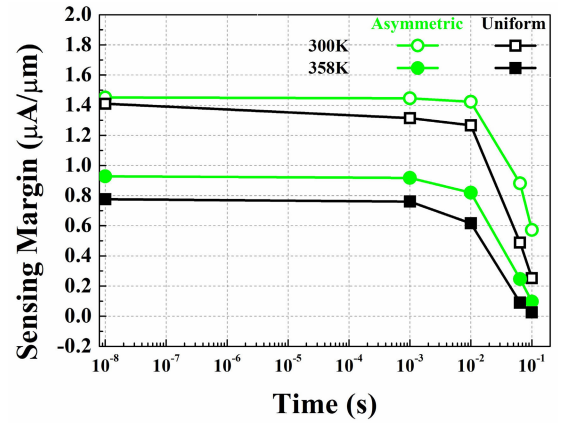


Fig. 9. Sensing margin and retention of asymmetric and uniform body 1T-DRAM at 300 and 358 K.

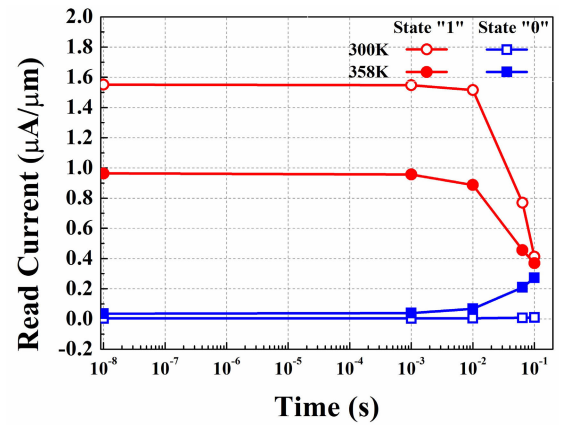


Fig. 10. Read current of asymmetric 1T-DRAM at 300 and 358 K.

retention time from 49 to 63 ms, as shown in Fig. 9. It was observed that the retention was 28.6% improved. In addition, it showed that the read current of state “1” decreased and the read current of state “0” increased in a higher temperature, as shown in Fig. 10. Recombination rate increased as temperature was higher and resulted in a lower sensing margin and retention time. Consequently, the sensing margin and retention decreased to $0.92 \mu\text{A}/\mu\text{m}$ and 42 ms at 358 K.

B. Double-Layered Structure

The double-layered structure was designed to increase the quantum well for a higher sensing margin. The body was separated vertically into two layers with a radius of 5 nm in different mole fractions. Since a higher mole fraction forms a larger quantum well, the mole fraction of the outer layer was 0.3. A simulation was preceded to decide the mole fraction of the inner and outer layer. Fig. 11 showed that hole carrier was concentrated in the center of the device after writing state “1.” It initiated strong recombination process, since the fully depleted body resulted in electrons flowing through the center of the body during read operation and recombination was proportional to excess carriers. Therefore, the sensing margin was 48.2% when the mole fraction of the inner layer was 0.3. As a result, the sensing margin was $5.12 \mu\text{A}/\mu\text{m}$ higher when mole fraction of the outer layer was 0.3, as shown in Fig. 8.

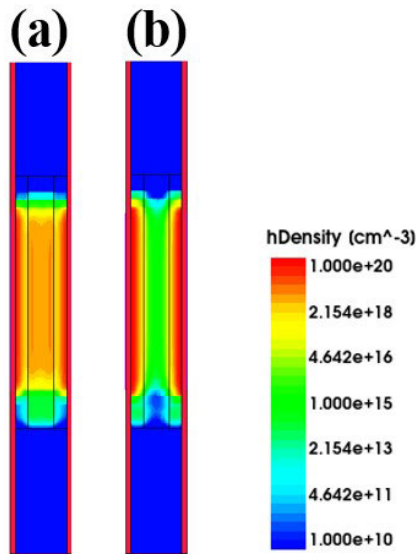


Fig. 11. Hole density of double-layered 1T-DRAM with $\text{Si}_{0.7}\text{Ge}_{0.3}$ (a) inner layer and (b) outer layer.

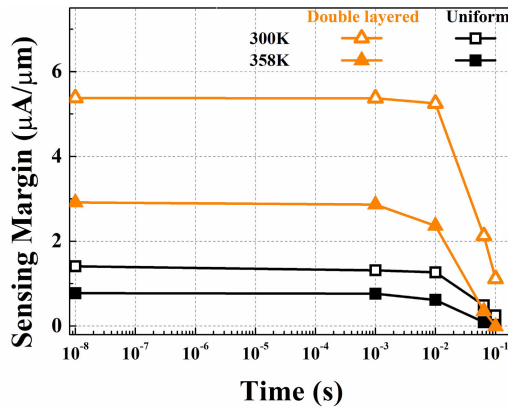


Fig. 12. Sensing margin and retention of double-layered and uniform 1T-DRAM.

The sensing margin increased significantly compared to the structure where the uniform body was $\text{Si}_{0.7}\text{Ge}_{0.3}$, as shown in Fig. 12. It was improved from 1.41 to $5.38 \mu\text{A}/\mu\text{m}$. Furthermore, the retention time increased from 50 to 54 ms as the underlap region was consisted of not only SiGe but also Si. It was possible to improve the sensing margin drastically, while the retention time was still under the JEDEC DDR4 standard, which is 64 ms [25].

C. Asymmetric Double-Layered Structure

The asymmetric double-layered structure was also proposed to improve the retention of a double-layered structure. Most of the recombination happened at the underlap region due to the strong internal electric field. Recombination process was accelerated in the narrow bandgap region. Since the underlap region of the outer layer in the double-layered structure had a relatively low energy band (0.99 eV) due to high mole fraction, the recombination rate was high resulting in the decrease of the retention time. Therefore, the asymmetric and double-layered structure was designed to improve the retention characteristics of the double-layered structure.

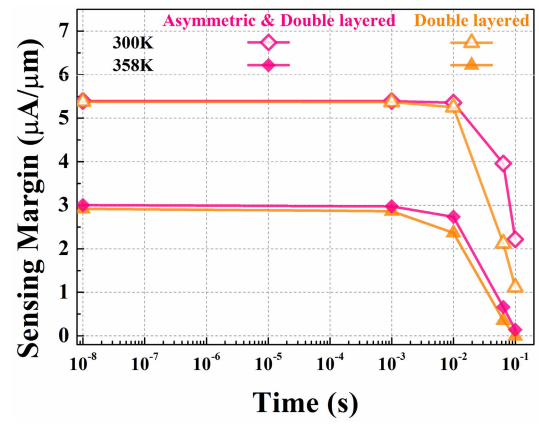


Fig. 13. Sensing margin and retention of double-layered and asymmetric double-layered 1T-DRAM.

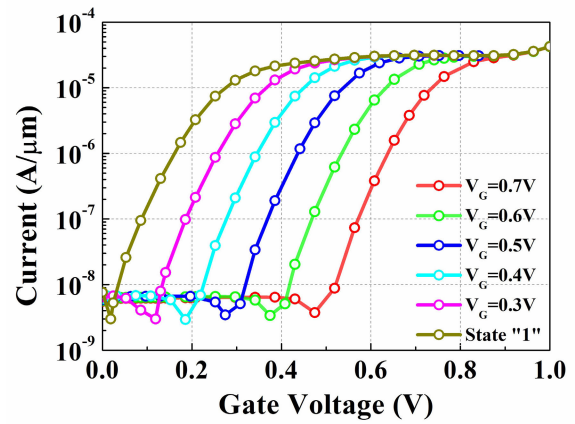


Fig. 14. Transfer curves of asymmetric double-layered 1T-DRAM after reading in different gate voltages.

Fig. 13 shows the comparison of the sensing margin and the retention time for double-layered and asymmetric and double layered structures. The retention time of the asymmetric and double-layered structure improved to 88 ms and it qualified the JEDEC standard while increasing the sensing margin up to $5.4 \mu\text{A}/\mu\text{m}$.

A simulation was additionally done to estimate the reliability of the device. Read operation was done twice continuously in order to check the destructivity of read operation. It turned out that ratio of the first and second reading current of state "1" was 59%. Fig. 14 shows the transfer curves after reading in different gate voltages. It showed that higher gate voltage decreased the amount of hole carriers gathered in the body and increased the threshold voltage. In fact, the ratio of the two reading currents of state "1" could be increased to 62.1% when the gate voltage was 0.5 V. However, destructiveness of the read operation was inevitable and refresh operation was required.

IV. CONCLUSION

Three body structures, such as asymmetric, double-layered, and asymmetric double-layered structures, were proposed to enhance the performances of a GAA JL-FET 1T-DRAM in the same scale. The asymmetric structure was to enhance the retention characteristics and the double-layered structure

was designed to enhance the sensing margin. The asymmetric and double-layered structure finally proposed to increase both characteristics up to $5.39 \mu\text{A}/\mu\text{m}$ and 88 ms.

It was observed that the three proposed structures improved the performance. However, the additional fabrication steps, such as additional trench steps for double-layered structure, are required. Even though the asymmetric double-layered structure had the highest sensing margin while qualifying the JEDEC standard, the process complexity was higher than the asymmetric structure. Performance and cost-efficiency must be considered for high-volume manufacturing. Furthermore, additional simulation related to reliability showed that most of the memory operation affected the characteristics of the device. Studies to relieve the destructive reading operation and disturbance of other operation should be required in the future for realistic manufacturing.

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